MODELING AND DESIGN OF ULTRA-LOW-VOLTAGE CMOS CIRCUITS

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10th IEEE Latin American Symposium on Circuits
Armenia – Colombia

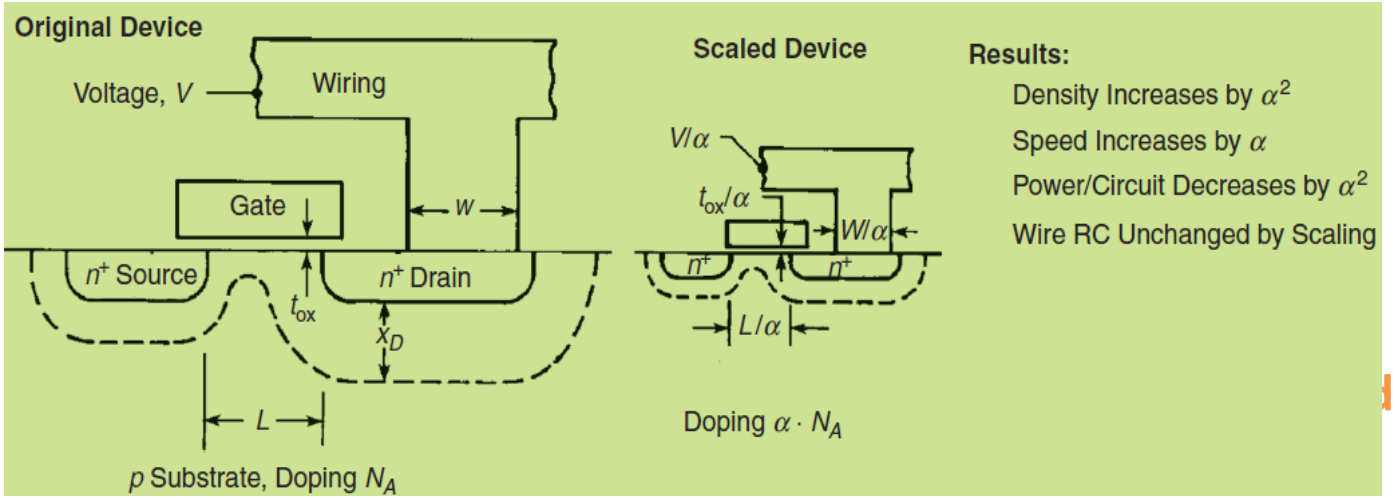
February 26, 2019

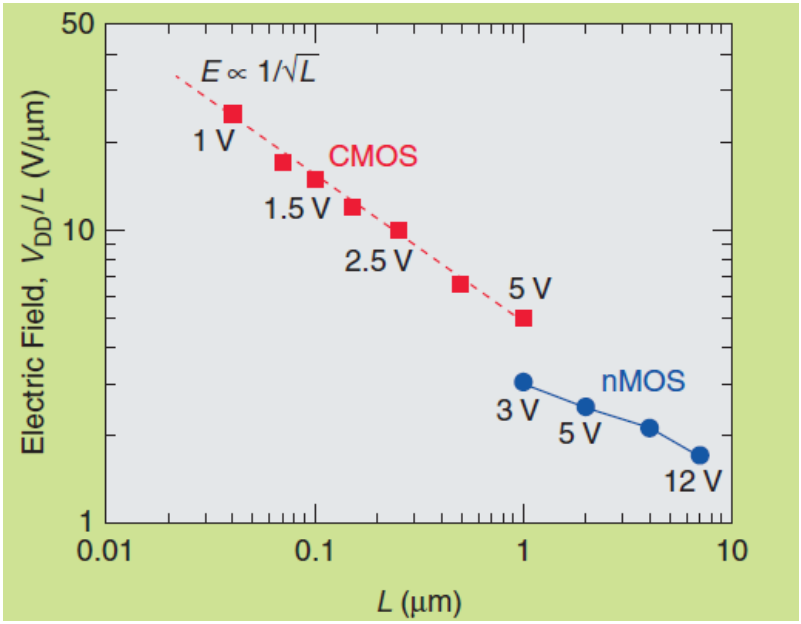
Outline

1. Introduction
2. All-region MOSFET model
3. Low-voltage CMOS digital circuits
4. Self-biased current source
5. Ultra-low-voltage (ULV) oscillators
6. ULV rectifiers & voltage multipliers

Motivations for low voltage

1. Scaling





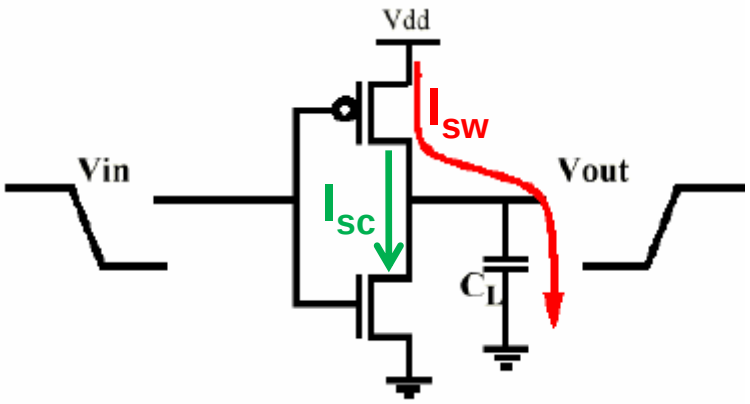
R. H. Dennard et et. al.
IEDM 72 & IEEE JSSC,
Oct. 1974

Motivations for low voltage

2. Power dissipation

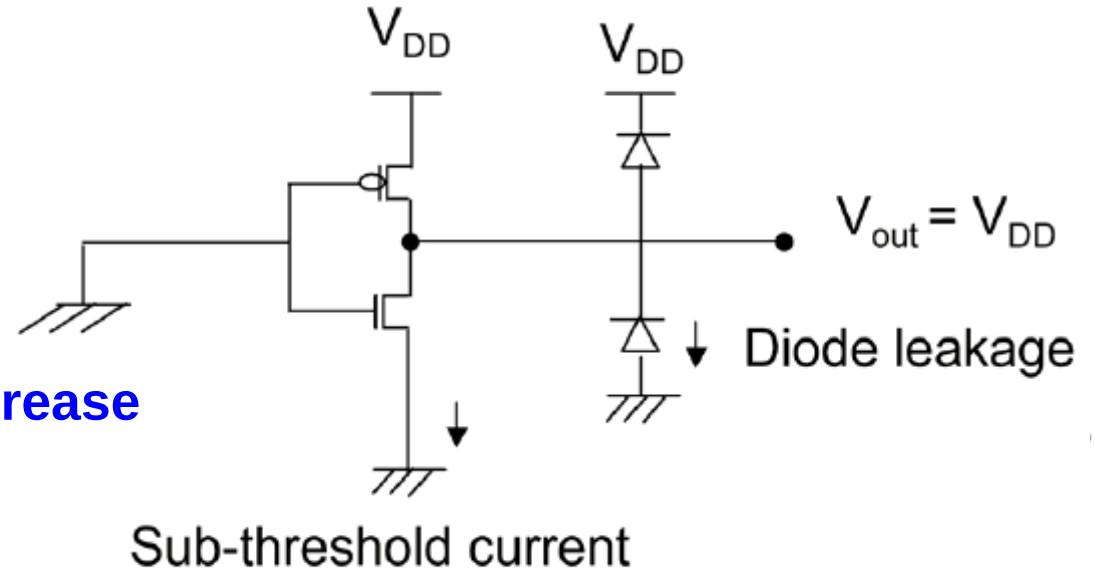
Switching power

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2$$



Short-circuit power :
due to non-zero rise/fall times

Leakage power α V_{DD}



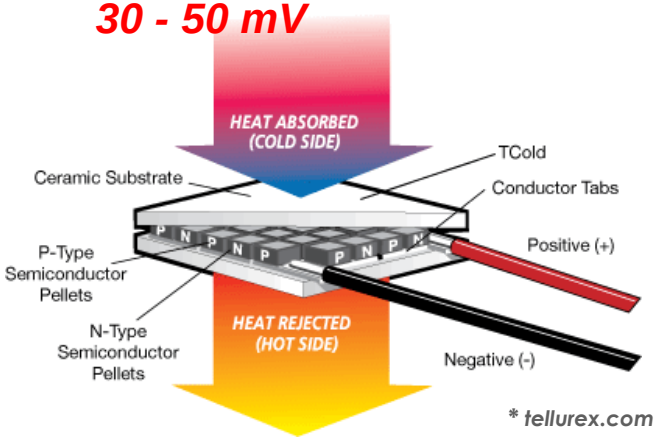
Most effective way to decrease power is to lower V_{DD}

Motivations for low voltage

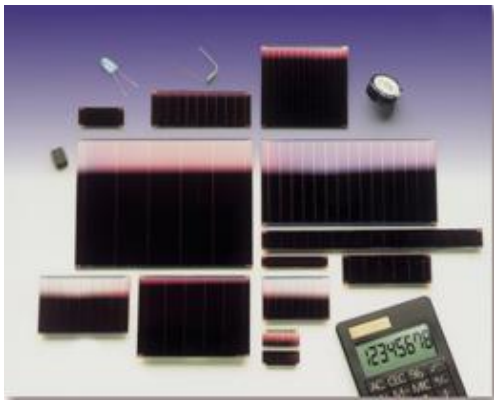
3. Low supply voltages

Thermoelectric generator

$V_{o(body\text{-}environment)} \approx$ *30 - 50 mV*



Photovoltaic cell

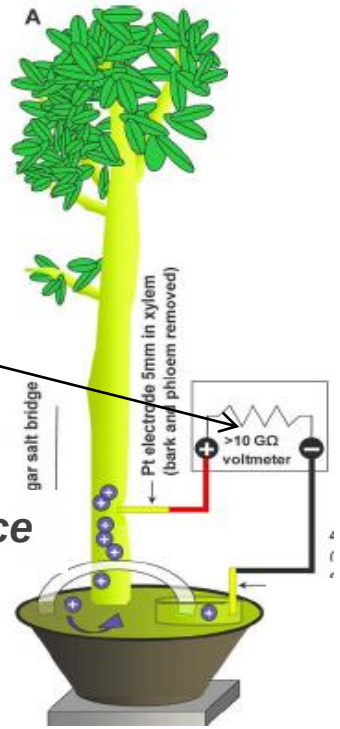


$V_{o(dark\ room)} \approx$ *100 - 200 mV*

Energy provided by trees

Vo ≈ 20-200 mV

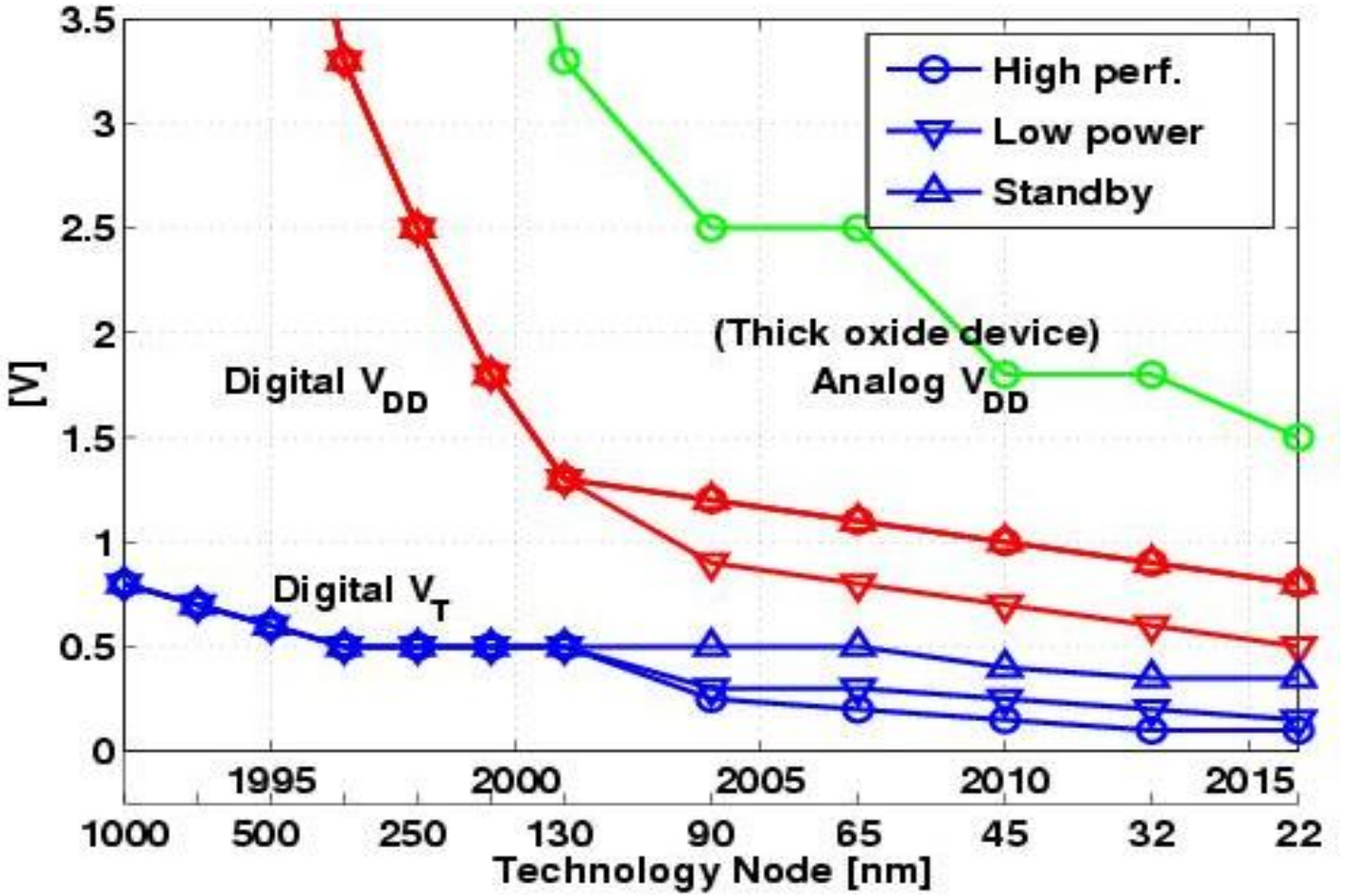
pH difference



** Love et al, "Source of sustained voltage difference between the xylem of a potted ficus benjamina tree and its soil", 2008.*

The trend toward low supply voltages

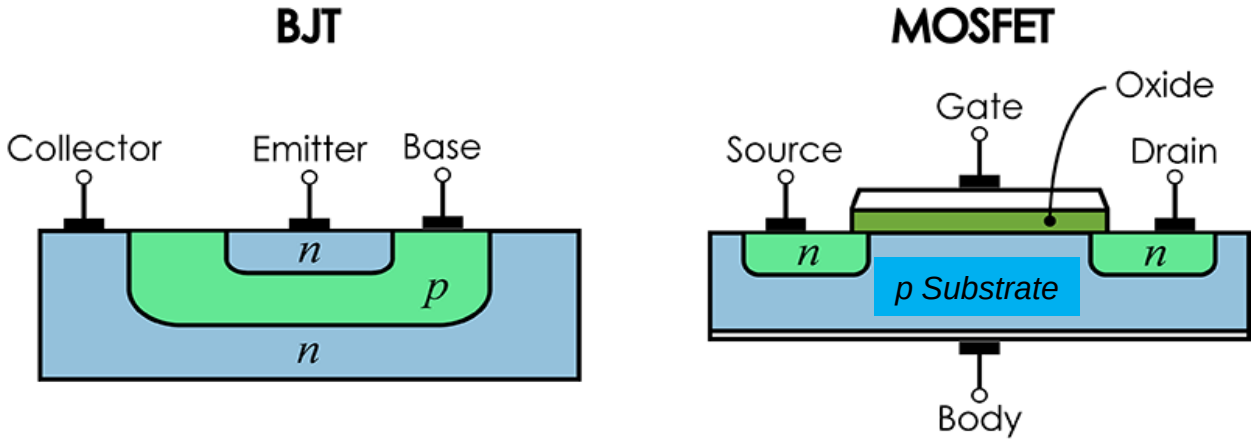
- Q1-Is there a lower bound for the supply voltage?
- Q2-What are the best technologies for ULV circuits?



Voltage scaling is slowing / stopping

http://www.cisl.columbia.edu/grads/tuku/research/

BJTs vs. MOSFETs: structural differences



BJT transconductance

$$g_m = \frac{\partial I_C}{\partial V_B}$$

Gate and source transconductances defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \qquad g_{ms} = -\frac{\partial I_D}{\partial V_S}$$

The body effect reduces the gate transconductance with respect to the source transconductance

$$g_m = \frac{g_{ms}}{n}$$

n ranges from ~ 1.1 to 1.5 in bulk technologies

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Weak and strong inversion models of the MOSFET

Weak inversion (WI) & saturation

$$I_{WI} = I_0 e^{V_G/n\phi_t} \quad \Rightarrow \quad I_{WI} = n g_m \phi_t$$

Strong inversion (SI)) & saturation

$$I_{SI} = \frac{1}{2n}\left(\mu C'_{ox}\frac{W}{L}\right)\left(V_G - V_{T0}\right)^2 \quad \Rightarrow \quad I_{SI} = \frac{n g_m^2}{2\mu C'_{ox}\left(W/L\right)}$$

V_{TO} is the threshold voltage at $V_{SB} = 0$

W/L is the aspect ratio, *μ is* the mobility and C'_{ox} is the oxide capacitance per unit area

All-region "interpolation" MOSFET model

$$I_{SI} = \frac{n g_m^2}{2\mu C'_{ox}\left(W/L\right)}$$

$$I_{WI} = n g_m \phi_t$$

for $g_m \to 0$ I_{SI} is negligible while for $g_m \to \infty$ I_{WI} is negligible.

$$I_D = I_{WI} + I_{SI} = n g_m \phi_t \left[1 + \frac{g_m}{2\mu C'_{ox}\phi_t \left(W/L\right)}\right]$$

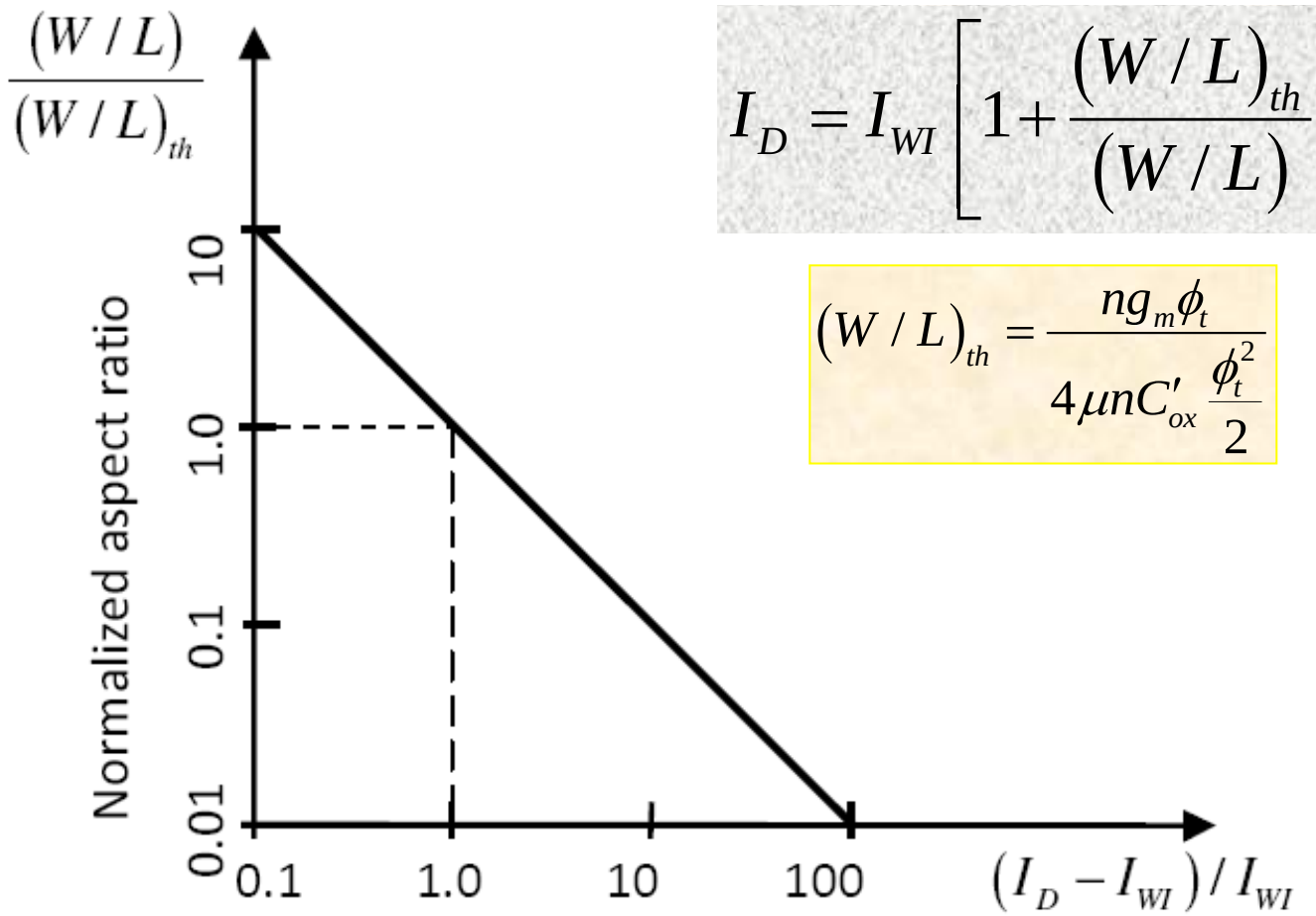
$$I_D = I_{WI}\left[1 + \frac{\left(W/L\right)_{th}}{\left(W/L\right)}\right]$$

$$g_m = \left(W/L\right)_{th} \mu\left(2C'_{ox}\phi_t\right)$$

Aspect ratio vs. current excess in MOSFET design

$$I_D = I_{WI}\left[1+\frac{(W/L)_{th}}{(W/L)}\right]$$

$$(W/L)_{th} = \frac{n g_m \phi_t}{4\mu n C'_{ox}\frac{\phi_t^2}{2}}$$



g_m/I_D model

$$I_D = n g_m \phi_t \left[1 + \frac{g_m}{2\mu C'_{ox} \phi_t (W/L)} \right] = n g_m \phi_t \left[1 + \frac{n g_m \phi_t}{4\mu n C'_{ox} \frac{\phi_t^2}{2} (W/L)} \right] \quad \textbf{(I)}$$

Defining the specific current I_S as $I_S = I_{SH}(W/L);\ I_{SH} = \mu n C'_{ox} \frac{\phi_t^2}{2}$

I_{SH} is the sheet specific current – technology parameter

the inversion level as $i_f = \frac{I_D}{I_S}$

i_f >> 1 strong inversion
i_f <<1 weak inversion

we rewrite (I) as

$$\frac{I_D}{n g_m \phi_t} = 1 + \frac{n g_m \phi_t i_f}{4 I_D} \quad \textbf{(II)}$$

and, with painless algebra

$$\frac{n g_m \phi_t}{I_D} = \frac{2}{1 + \sqrt{1 + i_f}} \quad \textbf{(III)}$$

The I-V MOSFET model (UICM)

Unified (I)current Control Model

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(1+\sqrt{1+i_f}\right)} \qquad g_m = \frac{g_{ms}}{n}$$

$$g_{ms} = -\frac{dI_D}{dV_S} = -I_S\frac{di_f}{dV_S} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f}-1\right) \Rightarrow -\frac{\phi_t}{2}\frac{di_f}{\sqrt{1+i_f}-1} = dV_S \quad \textbf{(I)}$$

Integrating (I) between V_S and V_P

$$V_P - V_S = \phi_t\left[\sqrt{1+i_f}-\sqrt{1+i_p}+\ln\left(\sqrt{1+i_f}-1\right)-\ln\left(\sqrt{1+i_p}-1\right)\right]$$

V_P is the pinch-off voltage

i_p is the normalized pinch-off drain current

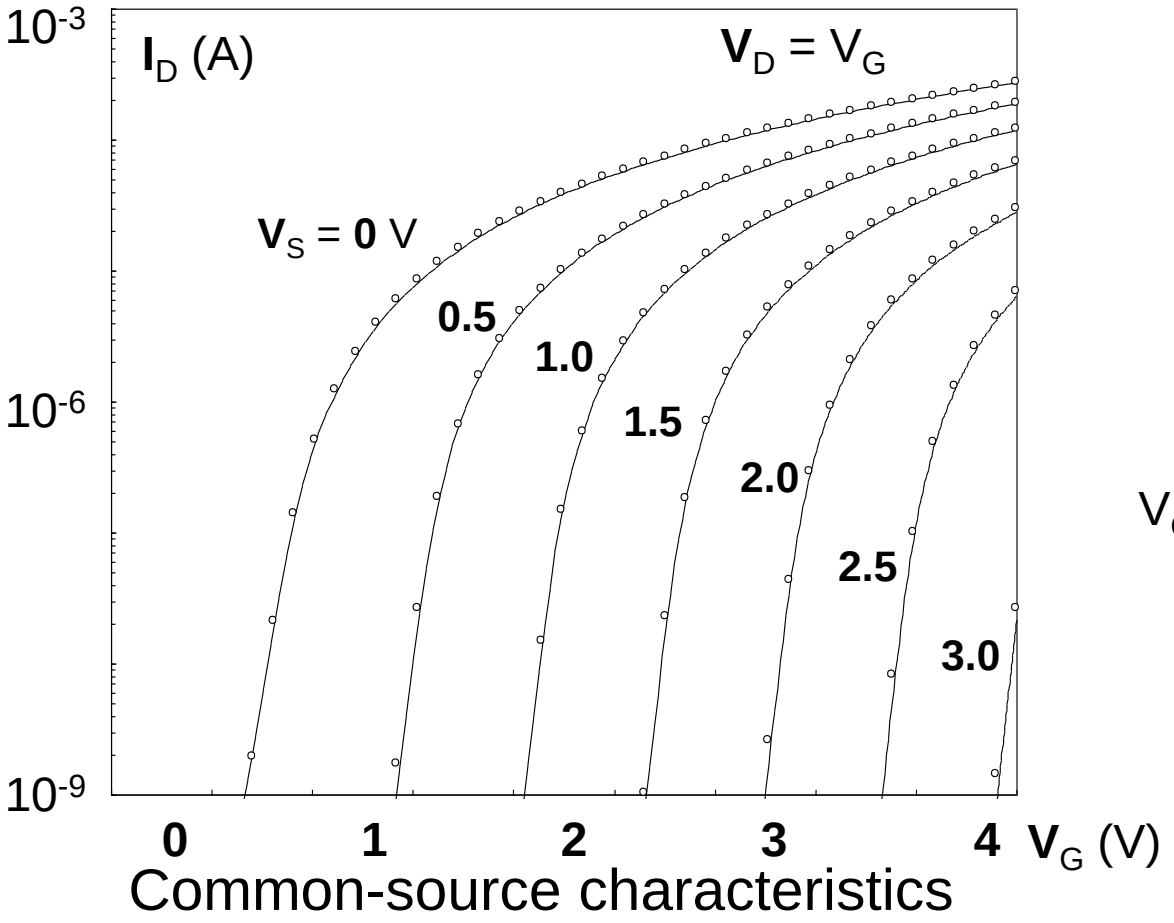
$$V_P \cong \frac{V_G - V_{T0}}{n}$$

Best choice i_p =3!

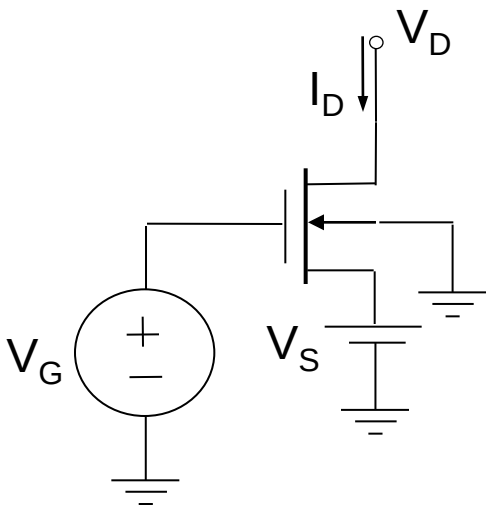
$$V_P - V_S = \phi_t\left[\sqrt{1+i_f}-2+\ln\left(\sqrt{1+i_f}-1\right)\right]$$

The I-V relationship for a saturated MOSFET

$$V_P - V_S = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right]$$



Common-source characteristics



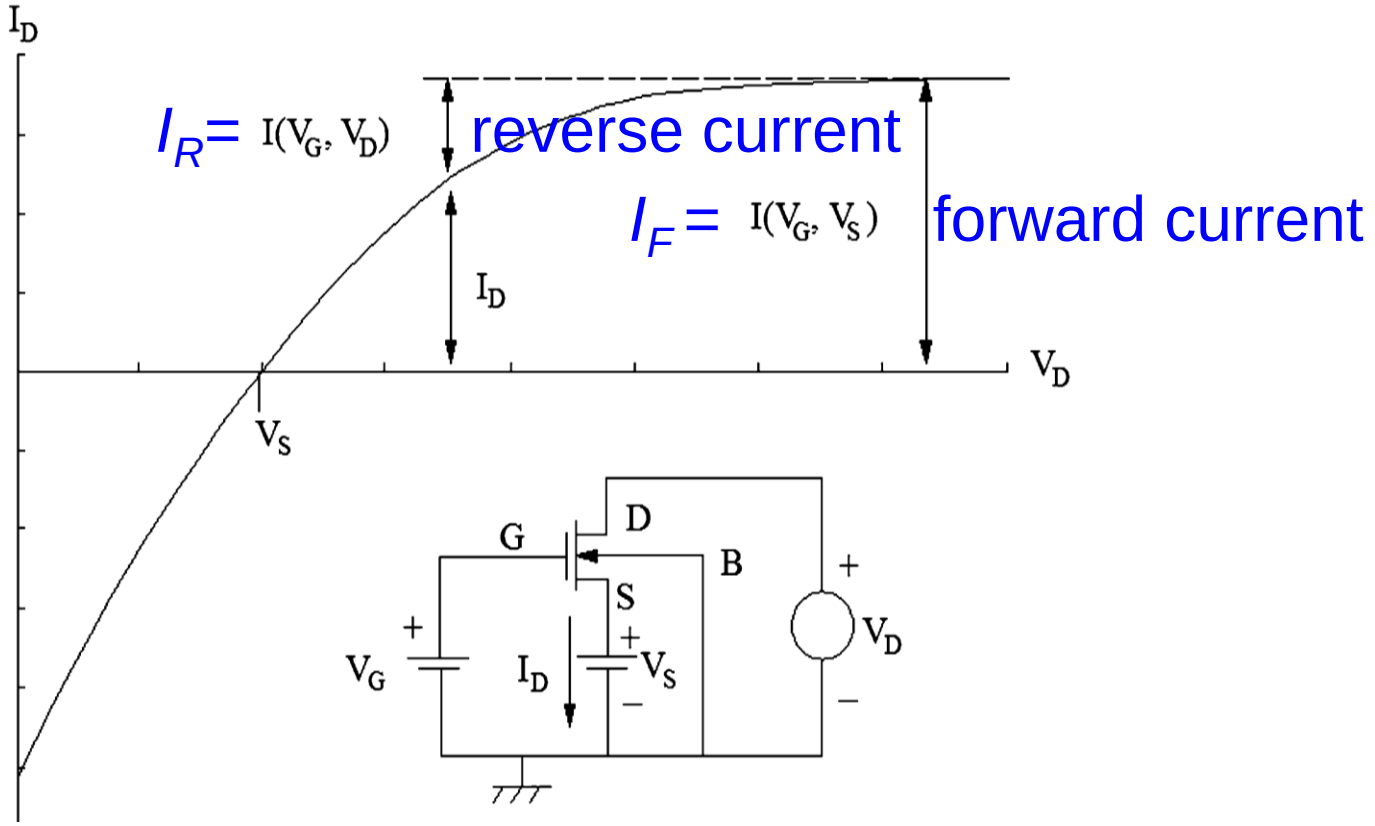
For *ideal* MOSFET → *n*=1 ⇨ $V_P - V_S = V_{GS} - V_{TO}$

Forward and reverse currents

Symmetry of the rectangular-geometry MOSFET

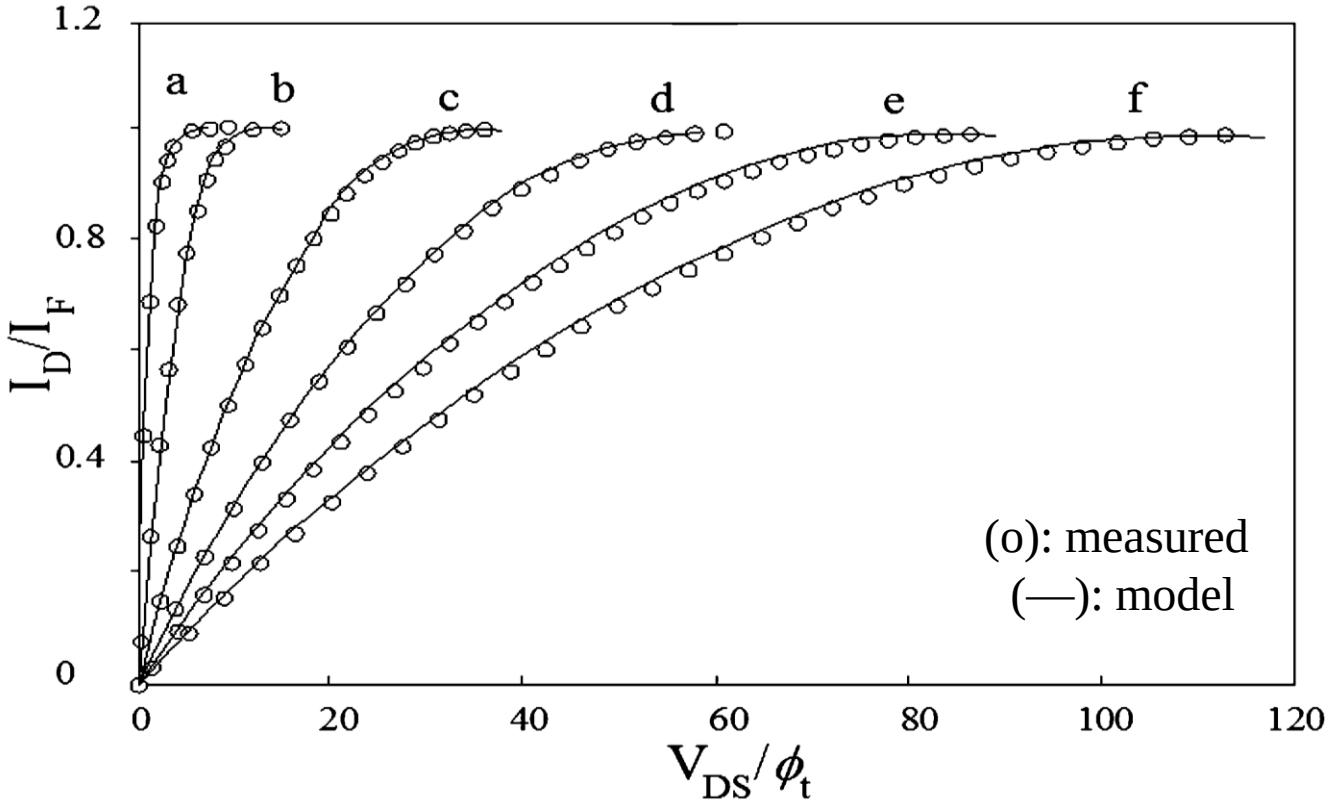
$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D)$$

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1 \right) \right]$$



Universal output characteristics

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)$$



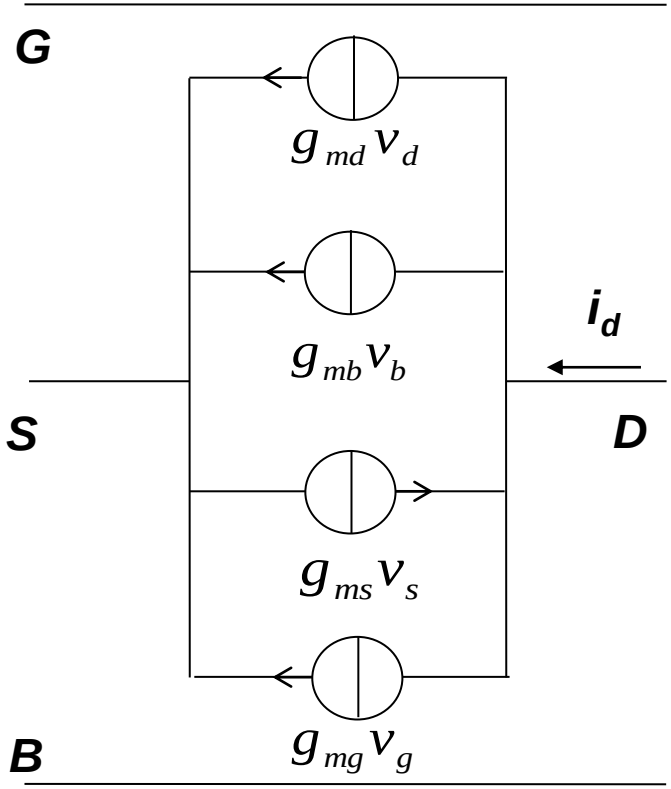
(a) i_f= 4.5x 10^{-2} (V_G=0.7 V); (b) i_f= 65(V_G= 1.2 V); (c) i_f= 9.5x10^2 (V_G= 2.0 V); (d) i_f= 3.1x 10^3 (V_G= 2.8 V); (e) i_f= 6.8x 10^3 (V_G= 3.6 V); (f) i_f= 1.2x 10^4 (V_G= 4.4 V).

Transconductances

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$$

$$g_{mg}(g_m) = \frac{\partial I_D}{\partial V_G}, g_{ms} = -\frac{\partial I_D}{\partial V_S}, g_{md} = \frac{\partial I_D}{\partial V_D}, g_{mb} = \frac{\partial I_D}{\partial V_B}$$

Low-frequency small-signal model



$$g_{mg} = \frac{g_{ms} - g_{md}}{n}$$

$$g_{mg} \cong \frac{g_{ms}}{n}$$

saturation

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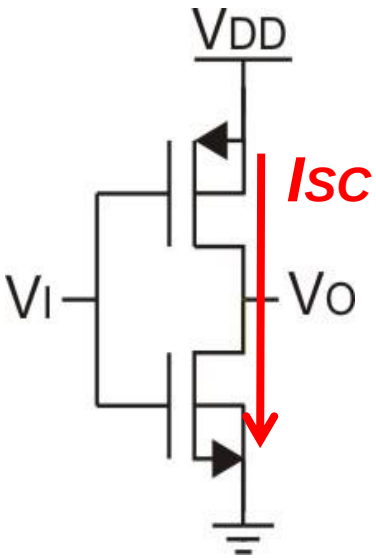
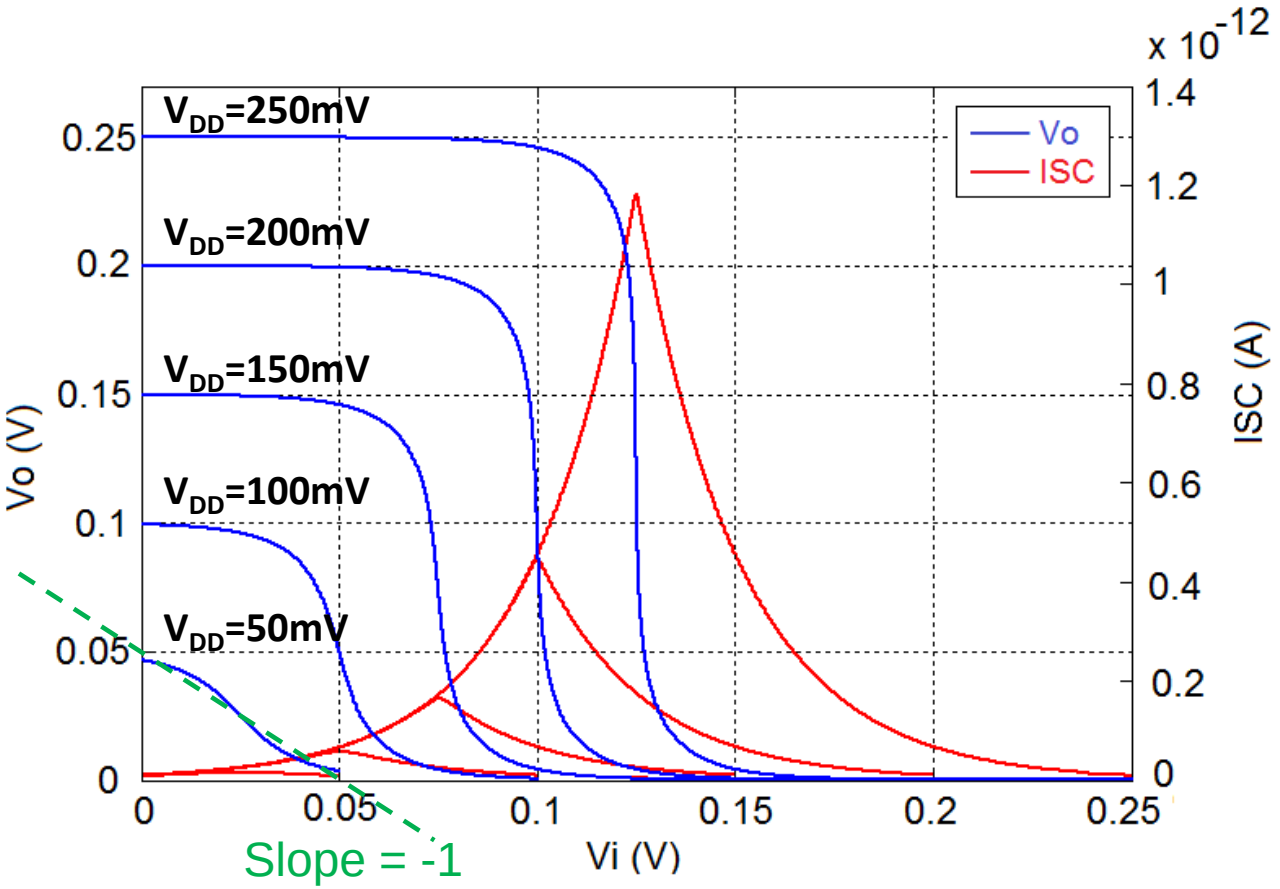
THE CMOS INVERTER IN WEAK INVERSION - 1

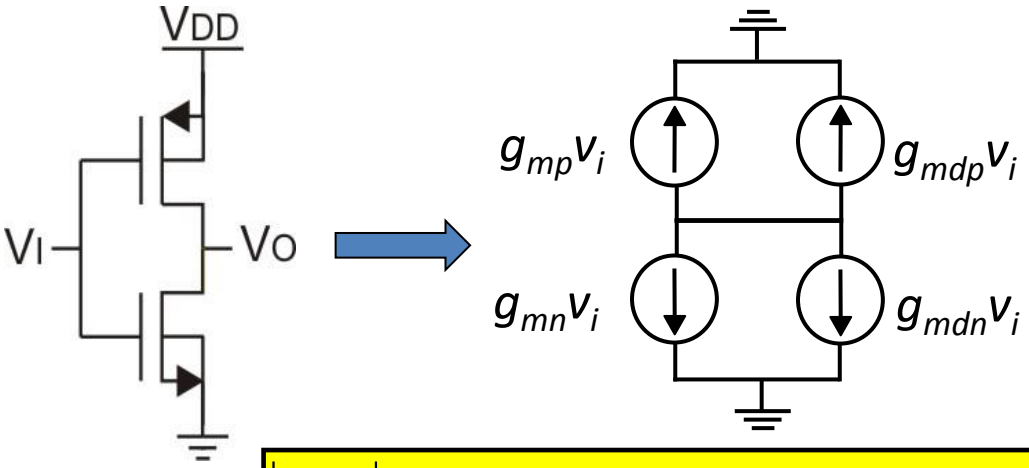




Note that:

VDD	VoH (Vi = 0)	VoL (Vi = VDD)
200 mV	200 mV	0mV
50 mV	46.6 mV	3.4mV

THE CMOS INVERTER IN WEAK INVERSION - 2



In the ideal case of NMOS and PMOS transistors with the same strength, and

$V_I=V_O=V_{DD}/2$

$g_{mdp}=g_{mdn}=g_{md}$

$g_{mp}=g_{mn}=g_m$

$$\left|\frac{dV_O}{dV_I}\right|_{V_I=V_O=\frac{V_{DD}}{2}}=\frac{g_m}{g_{md}}=\frac{1}{n}\frac{g_{ms}-g_{md}}{g_{md}}=\frac{1}{n}\left(e^{V_{DS}/\phi_t}-1\right)=\frac{1}{n}\left(e^{V_{DD}/2\phi_t}-1\right)$$

Regenerative logic → Minimum operating supply voltage of the CMOS static logic gate must be such that the voltage gain is, at least, equal to unity, *i.e.*

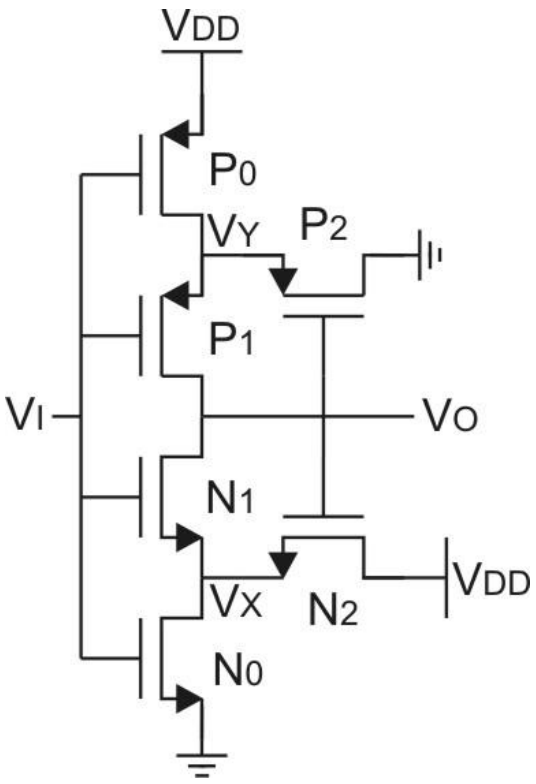
$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}}=\frac{1}{n}\left(e^{V_{DD}/2\phi_t}-1\right)=1$$

$$V_{DD\min}=2\phi_t\ln(2)$$

$$V_{DD\min}=36\text{ mV at }300\text{ K}$$

for *n*=1

The classic CMOS Schmitt trigger



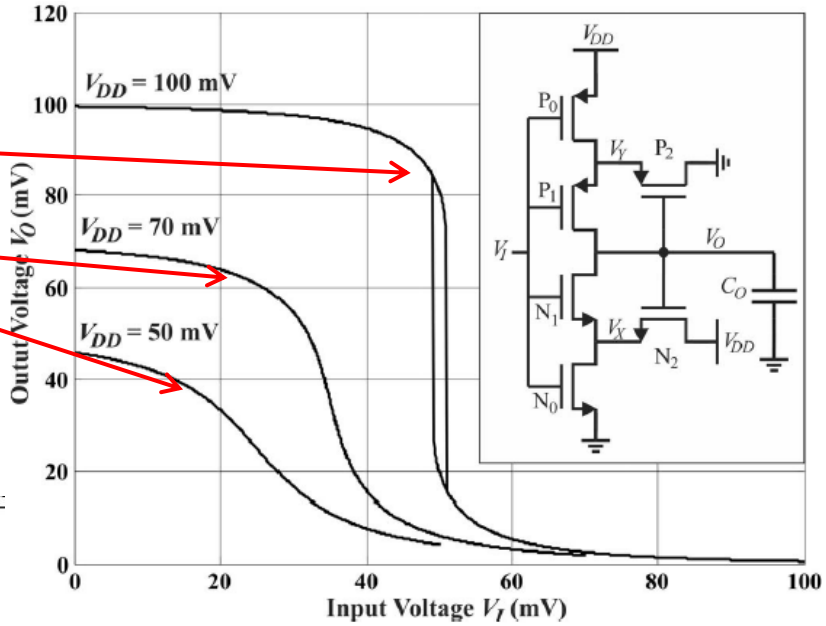
6-transistor Schmitt Trigger

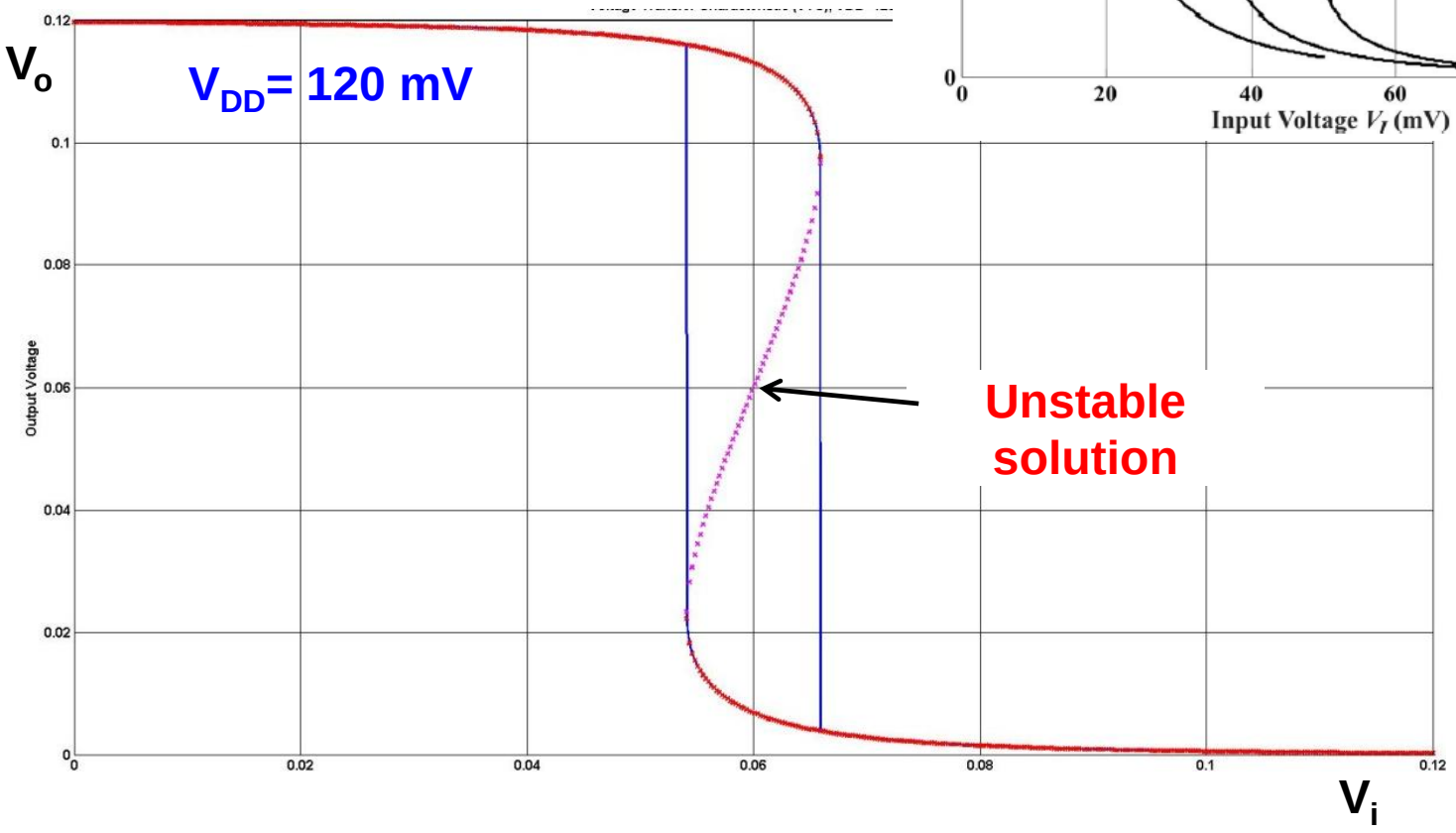
- *Positive feedback transistors (P2/N2) controlled by the output*
- *Modeled in strong inversion but not in weak inversion*
- *•For symmetric operation, corresponding NMOS and PMOS MOSFETs have the same current capability.*
- *Either gain improvement or hysteresis*
- *Logic from lower supply voltages*
- *Memory robustness ?*
- *Hysteresis dependent on VDD & relative transistor strength*

The 6-T Schmitt trigger

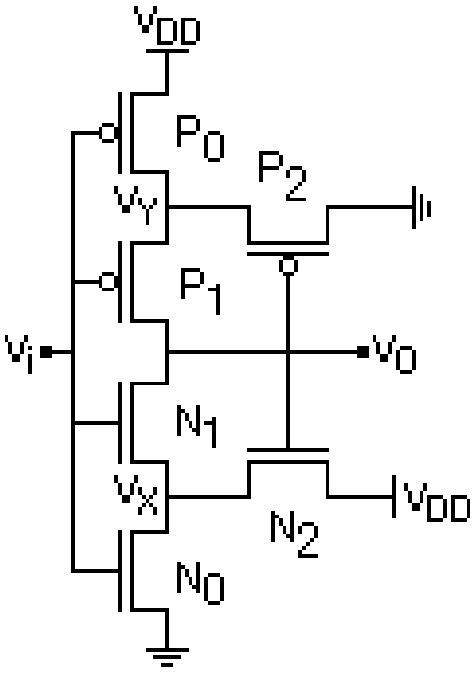
Hysteresis mode

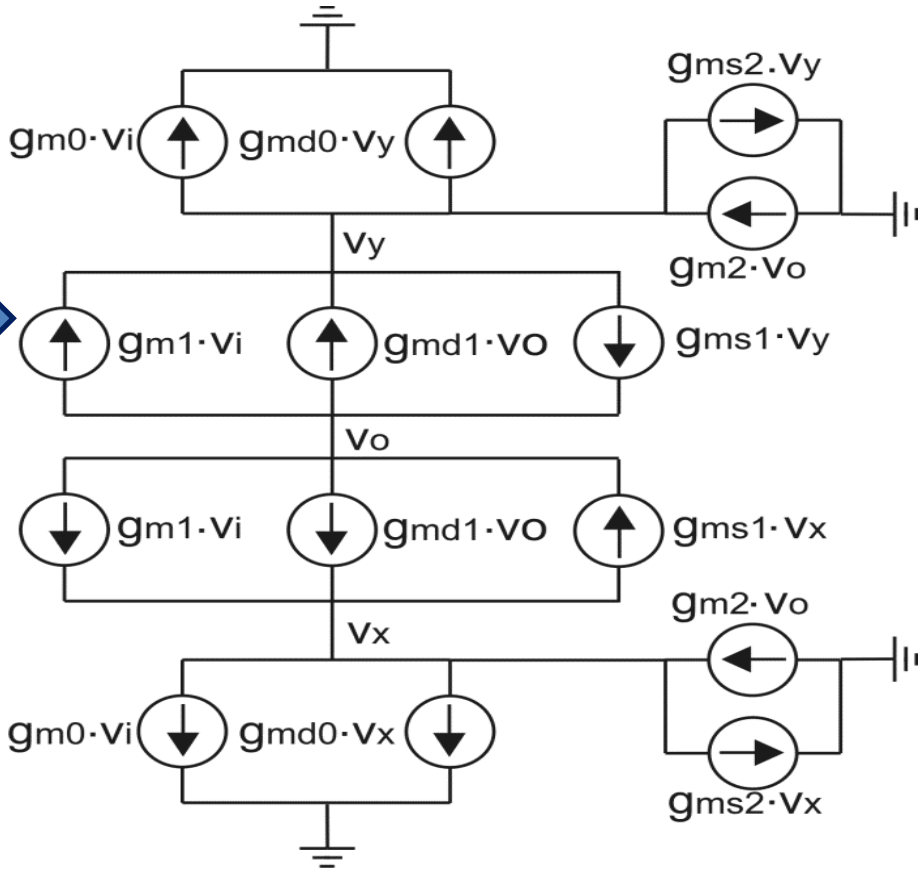
Amplifier mode





Schmitt Trigger small-signal model





$$A_{V,ST} = -\frac{g_{m1}}{g_{md1}} \frac{1+\dfrac{g_{ms1}g_{m0}}{g_{m1}\left(g_{ms2}+g_{md0}\right)}}{1-\dfrac{g_{ms1}g_{m2}}{g_{md1}\left(g_{ms2}+g_{md0}\right)}}$$

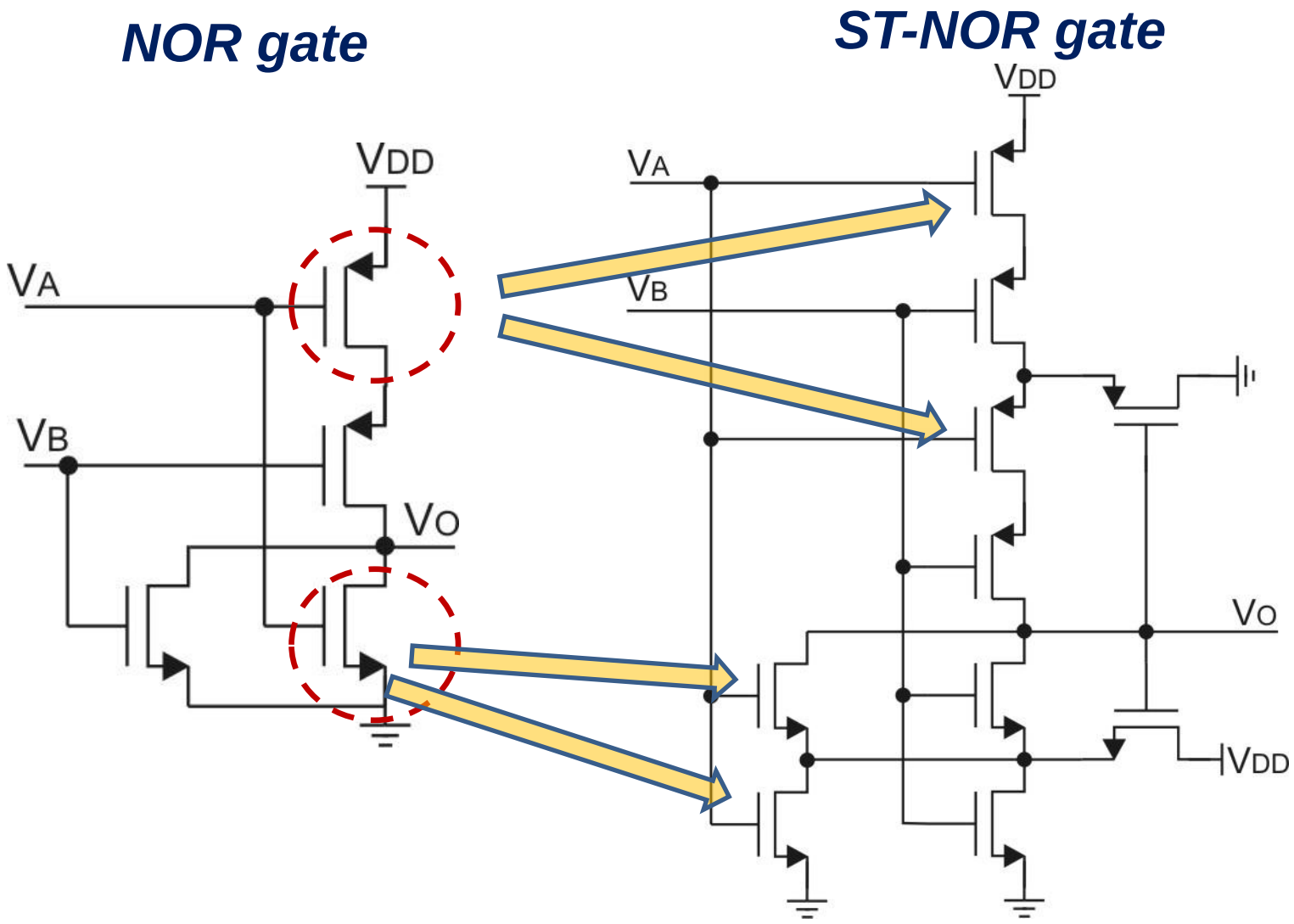
Voltage gain becomes ∞ for

$$V_{DD} \approx 2\phi_t \ln\left(2+\frac{I_0}{I_2}+\frac{I_2}{I_0}+\frac{I_1}{I_2}\right)$$

Supply voltage at which hysteresis starts to appear

Theoretical minimum: ~75 mV, but practical minimum ~100 mV

6-T Schmitt trigger logic



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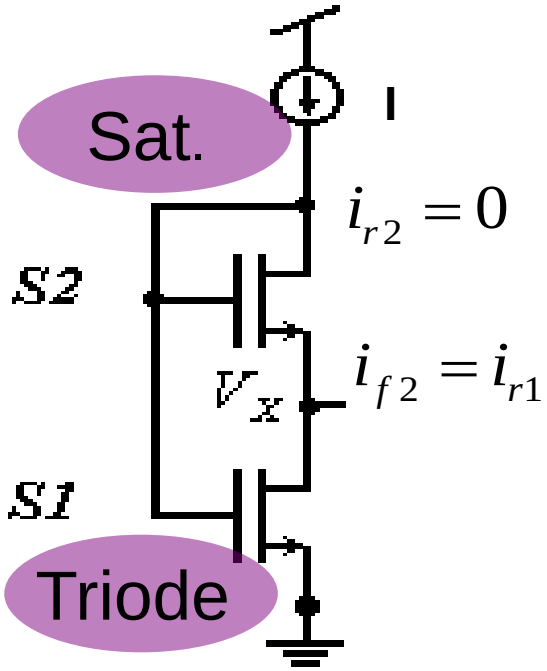
SELF-CASCODE MOSFET (SCM)



$$I = I_{S2} i_{f2} = I_{S1}(i_{f1} - i_{f2})$$

$$\Downarrow$$

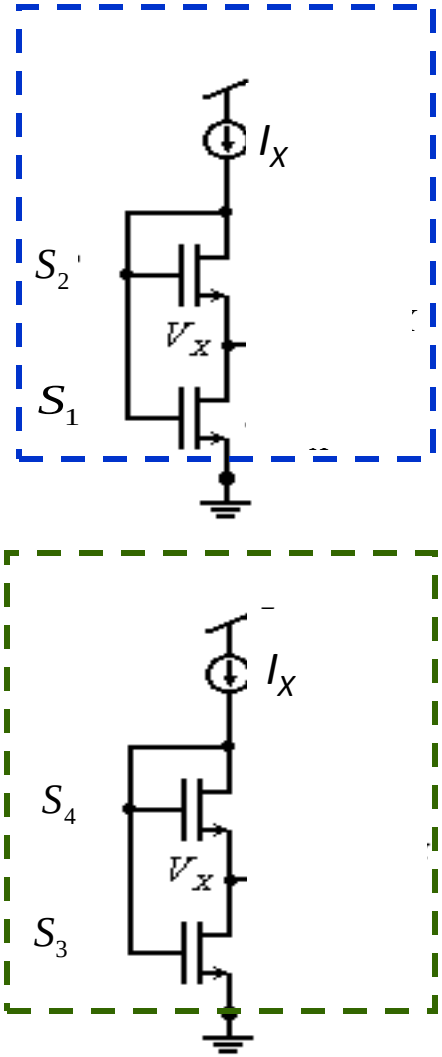
$$i_{f1} = \left(1 + \frac{I_{S2}}{I_{S1}}\right) i_{f2} = \left(1 + \frac{S_2}{S_1}\right) i_{f2} = \alpha i_{f2}$$

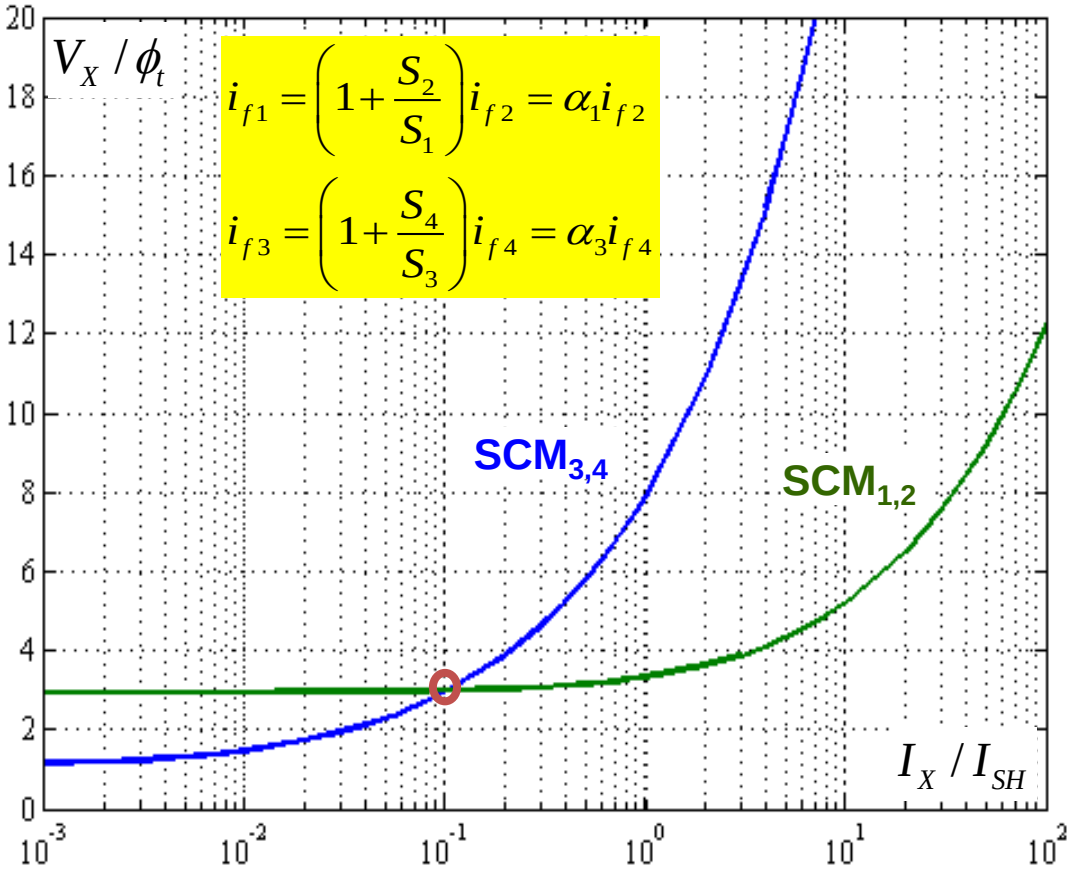
Applying UICM to M1

$$\frac{V_X}{\phi_t} = \sqrt{1+i_{f1}} - \sqrt{1+i_{f1}/\alpha} + \ln\left(\frac{\sqrt{1+i_{f1}}-1}{\sqrt{1+i_{f1}/\alpha}-1}\right)$$

In weak inversion, $i_{f1} << 1$ $\quad \frac{V_X}{\phi_t} \rightarrow \ln\alpha$

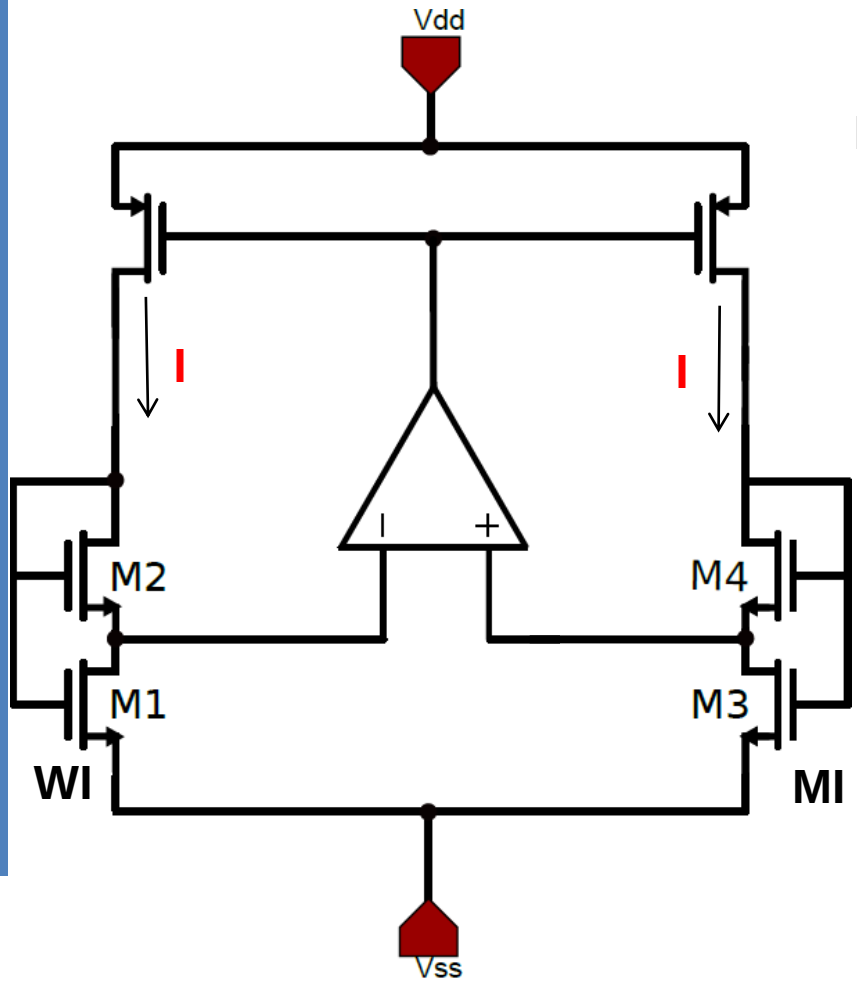
SELF-CASCODE MOSFETs (SCM)





Hypothesis: both S_2 & S_4 in saturation

Self biased current source (SBCS)



If V_{off} = 0 and M_1 and M_2 operate in WI it follows that

$$\ln \alpha_1 = \sqrt{1+i_{f3}} - \sqrt{1+i_{f3}/\alpha_3} + \ln\left(\frac{\sqrt{1+i_{f3}}-1}{\sqrt{1+i_{f3}/\alpha_3}-1}\right)$$

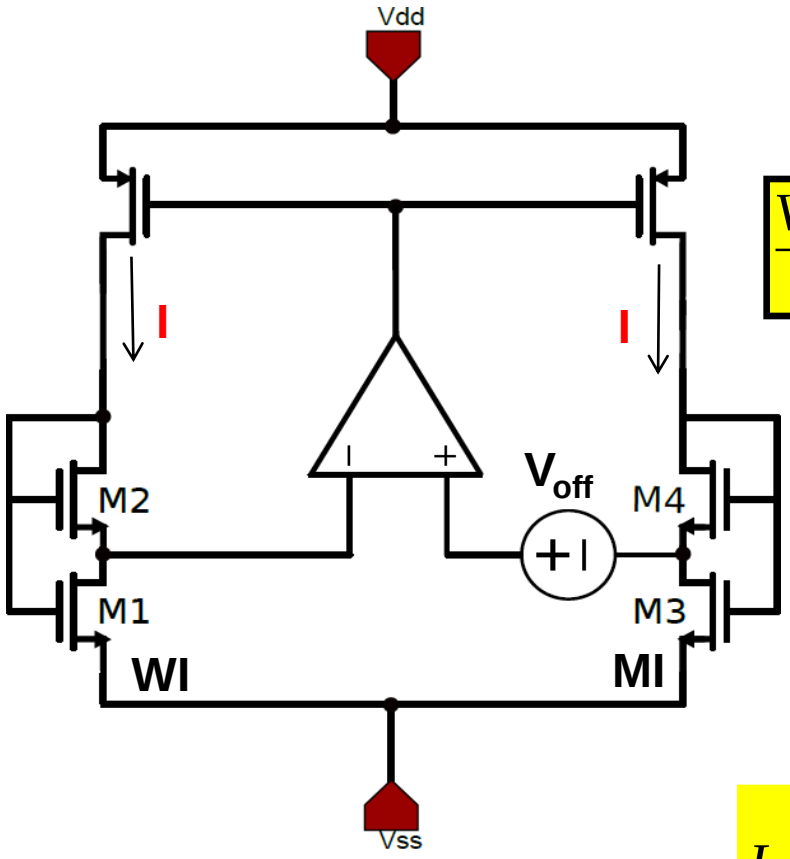
$$\alpha_1 = 1+\frac{S_2}{S_1} \qquad \alpha_3 = 1+\frac{S_4}{S_3}$$

$$i_{f4} = \frac{i_{f3}}{\alpha_3}$$

- **transistors are biased at constant inversion levels defined by aspect ratios, independent of technology & temperature**

Coupling two SCMs via an op amp and a current mirror

Using the SBCS for parameter extraction



Threshold voltage (VT) and specific current (IS) extractor

$$\frac{V_G - V_{T0}}{n} - V_S = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right]$$

$$V_S = 0 \Rightarrow V_G = V_{T0} \quad \text{for } i_f = 3$$

$i_{f3} = 3 \rightarrow V_{G3} = V_{T0}$

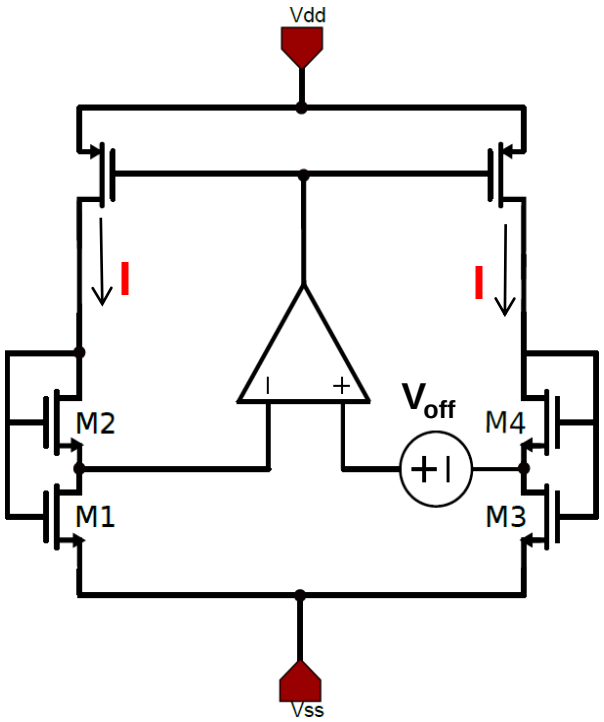
reference current

$I = I_{S4} i_{f4} = I_{S4} i_{f3} / (1 + S_4/S_3)$

$$I_S = I_{SH} (W/L); \quad I_{SH} = \mu n C'_{ox} \frac{\phi_t^2}{2}$$

- if mobility ~ T^{-1}, then $I \sim I_{S4}$ is PTAT

Inaccuracy of the SI approximation



Assuming M3 in SI in the linear region
(equivalent to a resistor)

$$i_{f3} \approx \frac{\alpha_3 \ln^2 \alpha_1}{\left(\sqrt{\alpha_3} - 1\right)^2} \approx 4\left(\frac{S_3}{S_4}\right)^2 \ln^2 \alpha_1$$

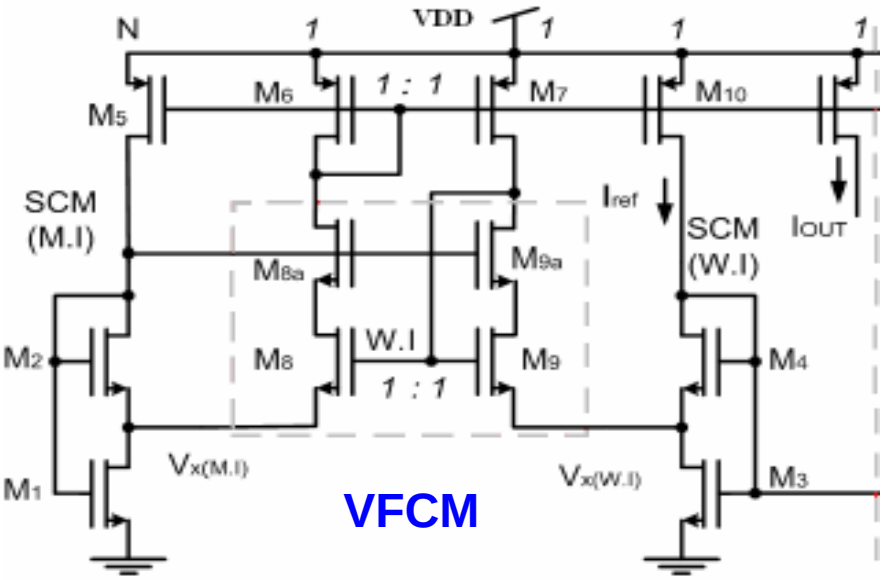
E. A. Vittoz, CCCD Workshop, Lund, 2003.

For $\ln\alpha_1 = 4$ (practical maximum value)

S_3/S_4	i_{f3} [1]	i_{f3} [2]	$V_{GS}-V_{T0}$ (n = 1.2, V_{BS} = 0, T = 300K)
10	6400	7200	2.57 V
2.5	400	610	0.65 V

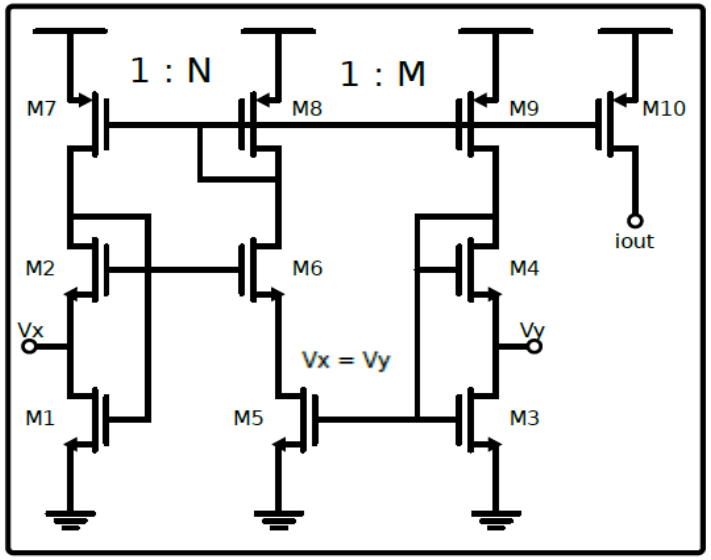
[1] Strong inversion model. [2] Accurate all-region MOSFET model

Variations of the SBCS topology

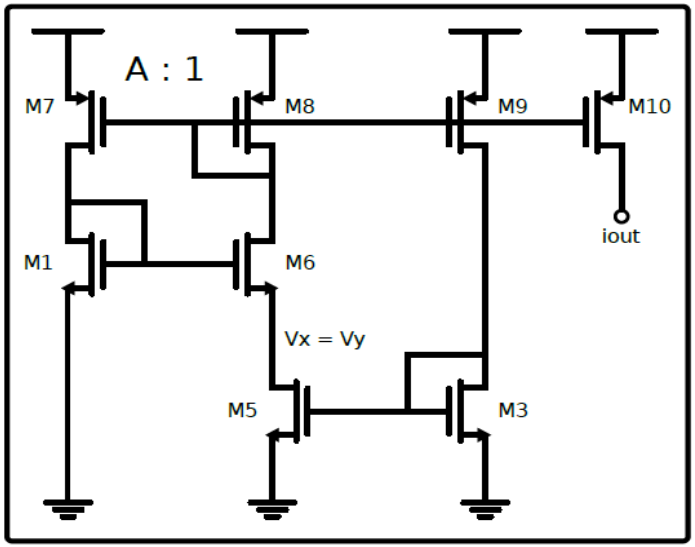


Coupling two SCMs via a Voltage-Following Current Mirror

E. M. Camacho-Galeano, C. Galup-Montoro and M. C. Schneider, "A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology", IEEE Trans. Circ. Syst. II, February 2005



P. Heim, S. Schultz, and M. A. Jabri, *4th IEEE International Workshop on Cellular Neural Networks and their Applications (CNNA-95),* 1995.



H. J. Oguey and D. Aebischer, *IEEE J. Solid-State Circuits*, July 1997.

Outline

1. Introduction
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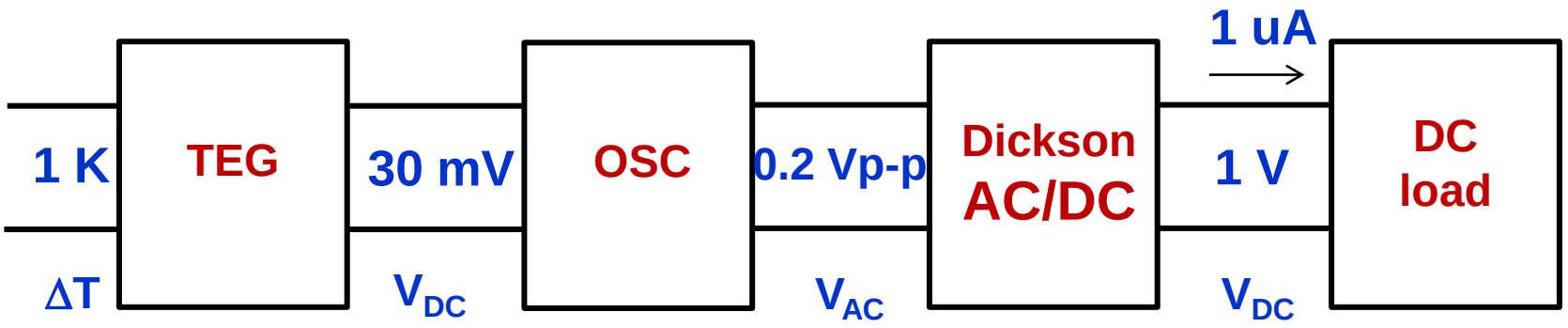
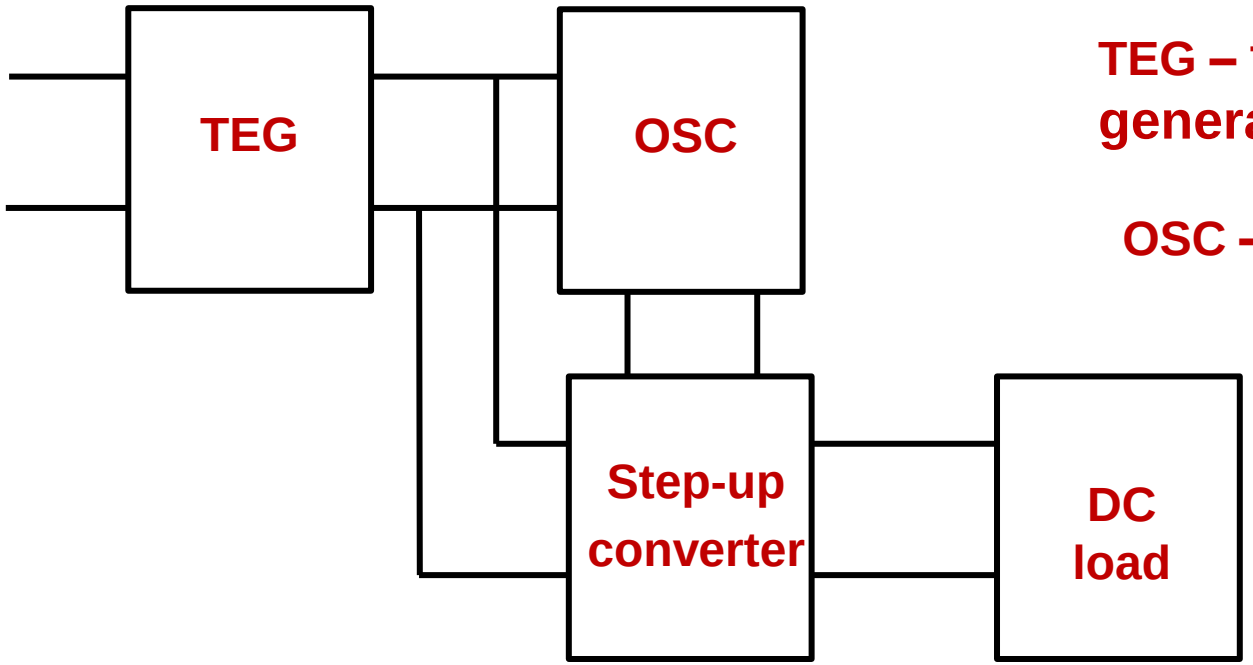
4. Self-biased current source
5. Ultra-low-voltage (ULV) oscillators
6. ULV rectifiers & voltage multipliers

Application of ULV oscillators in energy harvesters

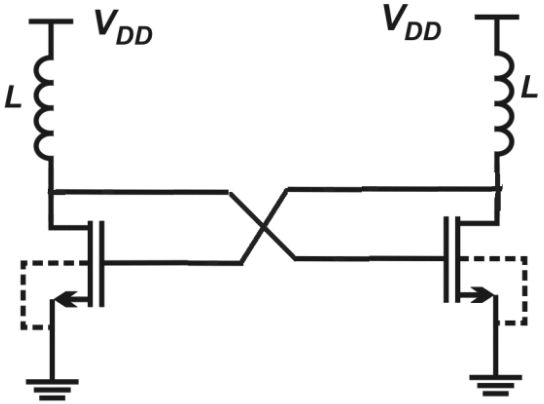




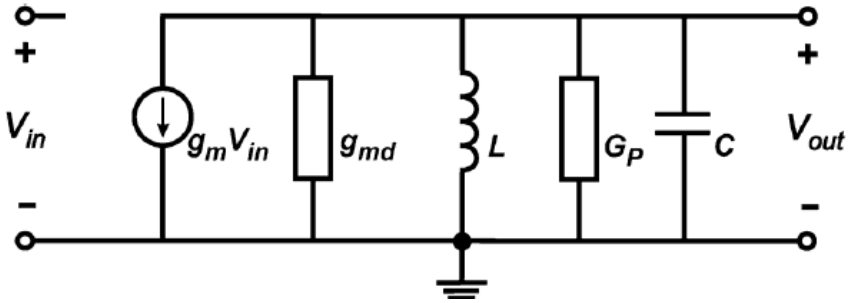
TEG – thermoelectric generator

OSC – oscillator

Inductive ring (X-coupled) oscillator - 1



Cross-coupled LC oscillator



$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi} \quad \text{=–1}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L(g_{md}+G_p)}$$

Criterion for oscillation (Barkhausen)

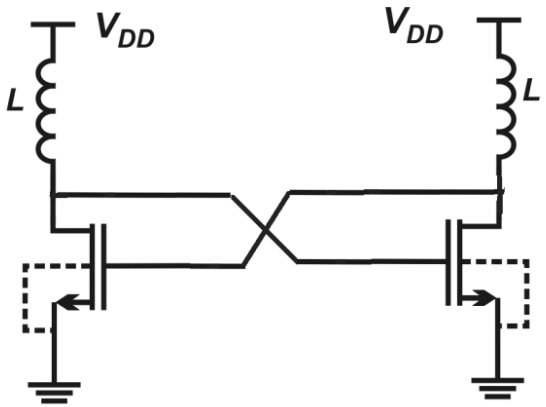
ϕ=0 & V_{out}/V_{in}=-1

$$\omega^2 LC = 1$$

$$\frac{g_m}{g_{md}+G_P} = 1$$

What´s the minimum V_{DD} for oscillation?

Inductive ring oscillator - 2



Cross-coupled LC oscillator

Oscillation frequency $\omega^2 LC = 1$

Voltage gain $\dfrac{g_m}{g_{md} + G_P} = 1$

What´s the minimum V_{DD} for oscillation?

Recall that $g_m = \dfrac{g_{ms} - g_{md}}{n}$

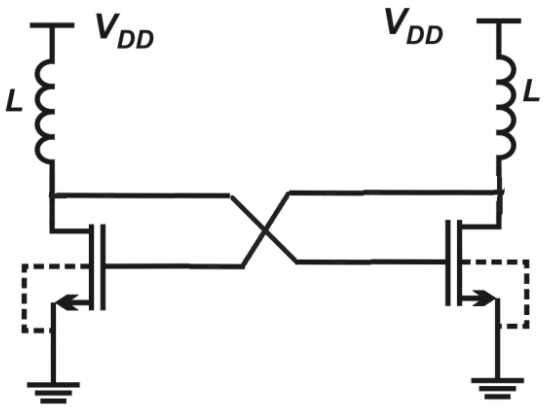
Voltage gain=1 ⇒ (i) $\dfrac{g_{ms}}{g_{md}} = 1 + n\left(1 + \dfrac{G_P}{g_{md}}\right)$

In weak inversion ⇒ (ii) $\dfrac{g_{ms}}{g_{md}} = e^{V_{DS}/\varphi_t} = e^{V_{DD}/\varphi_t}$ since $V_G = V_D = V_{DD}$

$$V_{DD,\min} = \varphi_t \ln\left[1 + n\left(1 + \frac{G_P}{g_{md}}\right)\right] = \varphi_t \ln\left[1 + n\right] \quad \text{for} \quad \frac{G_P}{g_{md}} << 1$$

Similar to the result (/2) of the CMOS inverter

Inductive ring oscillator - 3

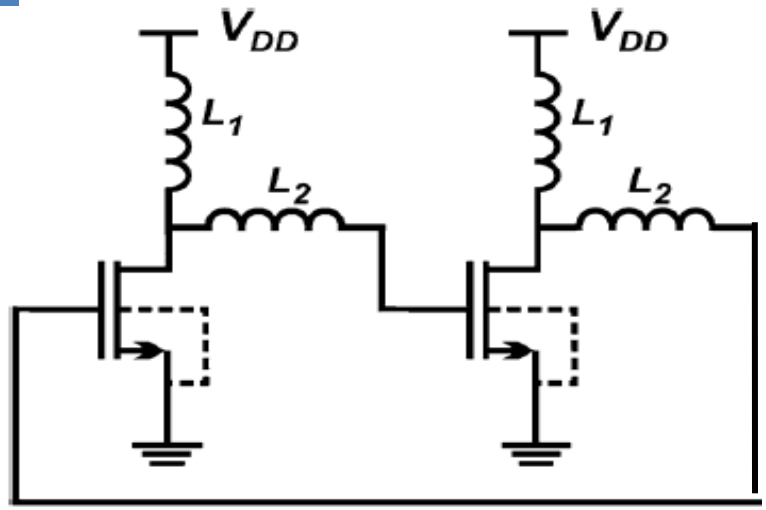


Questions:

1. How to reduce $V_{DD,min}$?

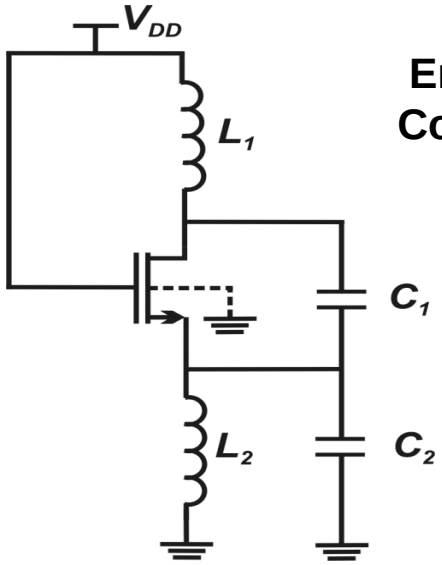
2. How to increase the V_{DD}-limited voltage swing?

Introduce voltage gain from drain to gate



Enhanced swing IRO (ESRO)

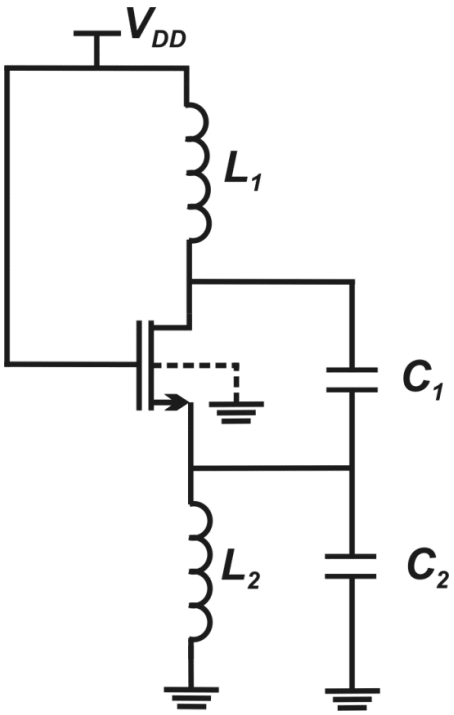
Change topology, e. g., take advantage of CG gain

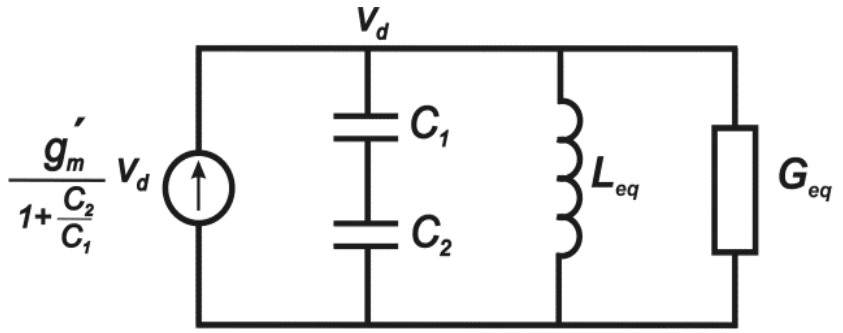


Enhanced swing Colpitts oscillator (ESCO) *

* T. W. Brown et al, *IEEE JSSC*, Aug. 2011.

The enhanced-swing Colpitts oscillator (ESCO)





$$G_{eq} = G_1 + \left(\frac{C_1}{C_1+C_2}\right)^2 (G_2+g_m') \qquad \frac{1}{L_{eq}} = \frac{1}{L_1} + \left(\frac{C_1}{C_1+C_2}\right)^2 \frac{1}{L_2}$$

$$v_s \cong \frac{v_d}{1+\frac{C_2}{C_1}} \rightarrow g_{ms}v_s - g_{md}v_d \cong g_m'v_s \qquad g_m' = g_{ms} - \left(1+\frac{C_2}{C_1}\right)g_{md}$$

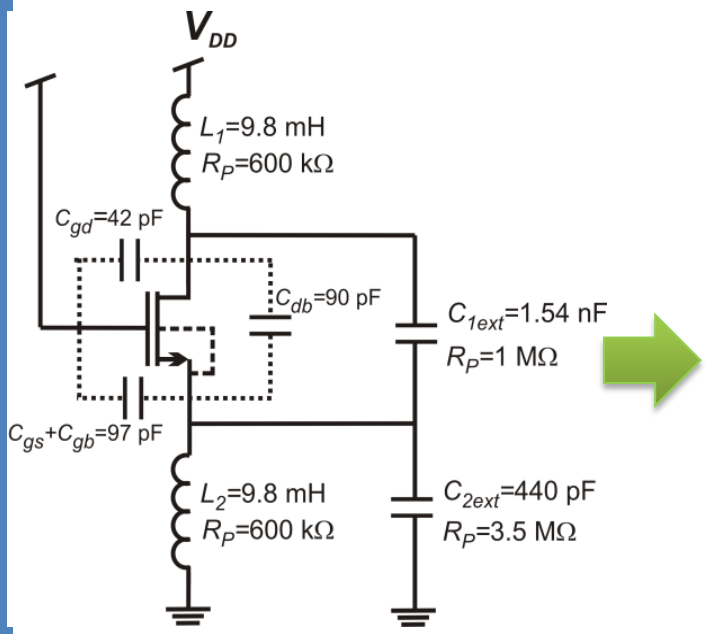
For lossless inductors and capacitors

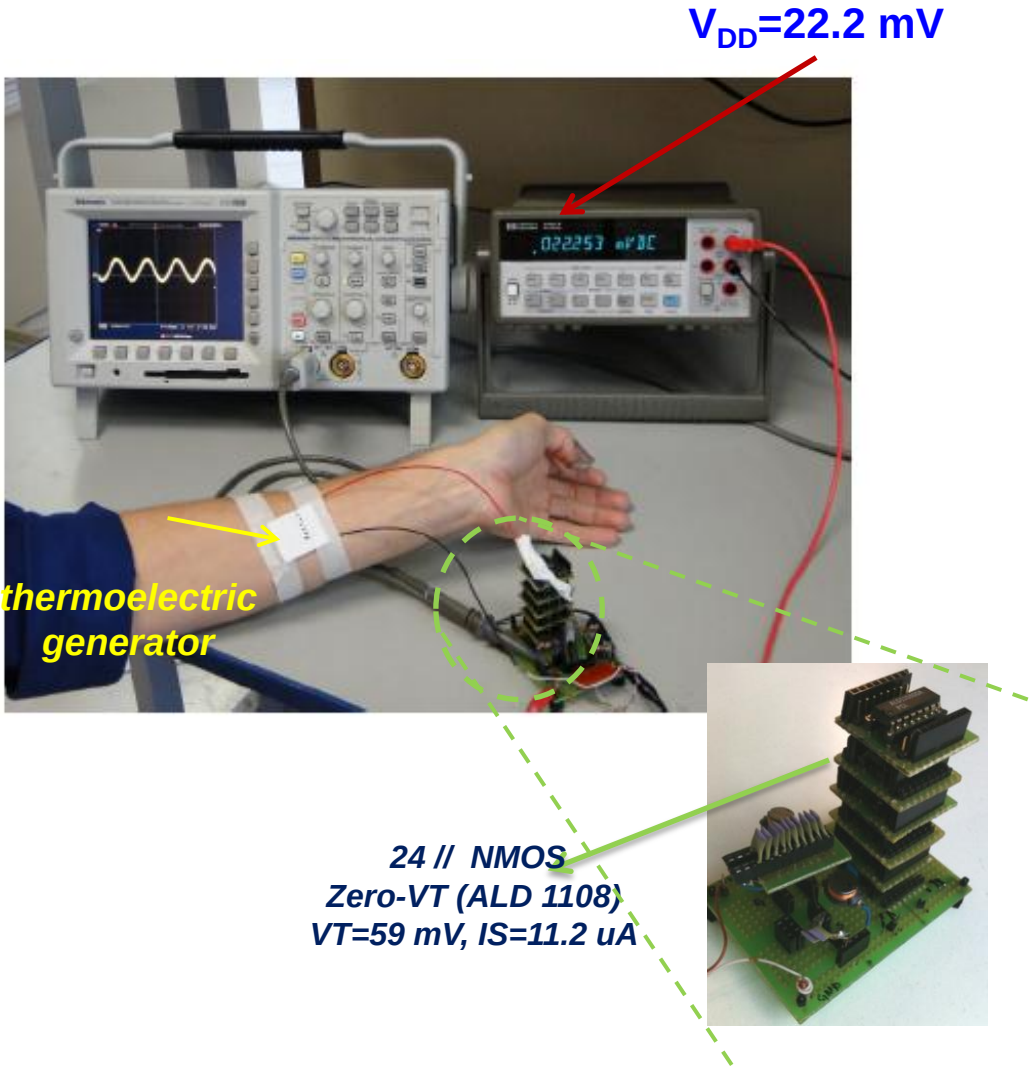
Weak inversion

$$V_{DD\lim} = \frac{kT}{q}\ln\left(1+\frac{C_2}{C_1}\right)$$

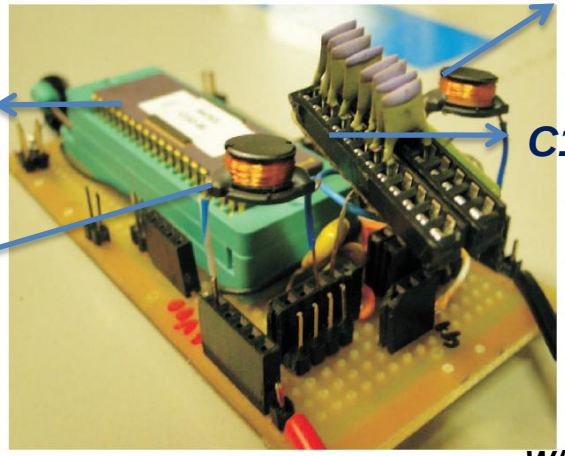
Colpitts oscillator: first prototype

Off-the-shelf components

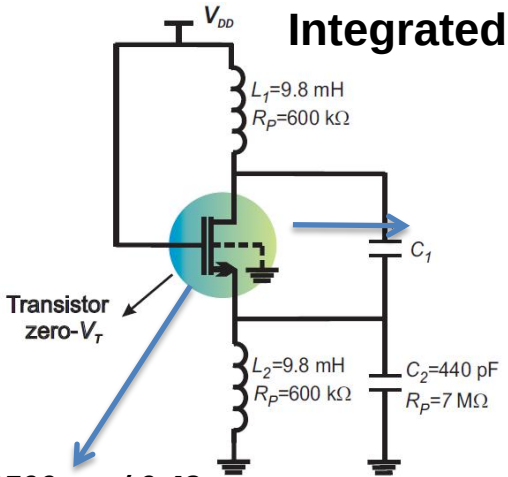




Colpitts oscillator: second prototype

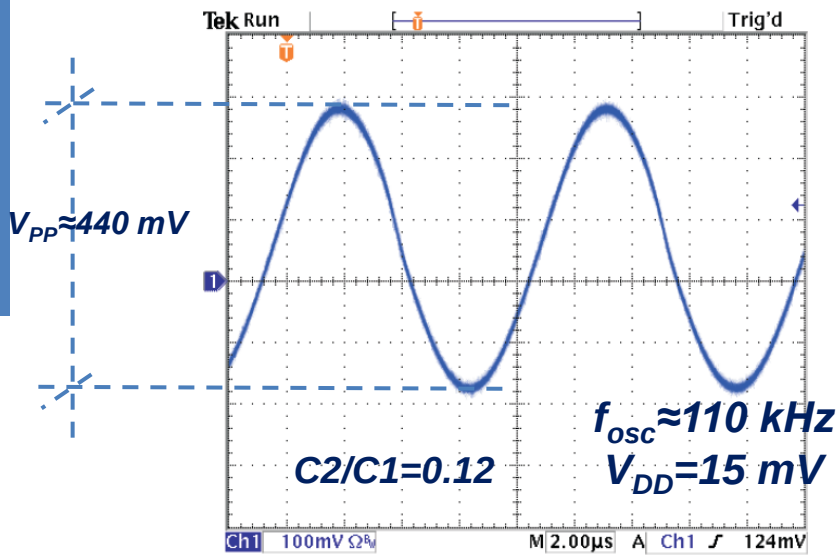


Zero-VT
IBM 130 nm



Integrated Zero-VT MOSFET

W/L = 2500 µm / 0.42 µm

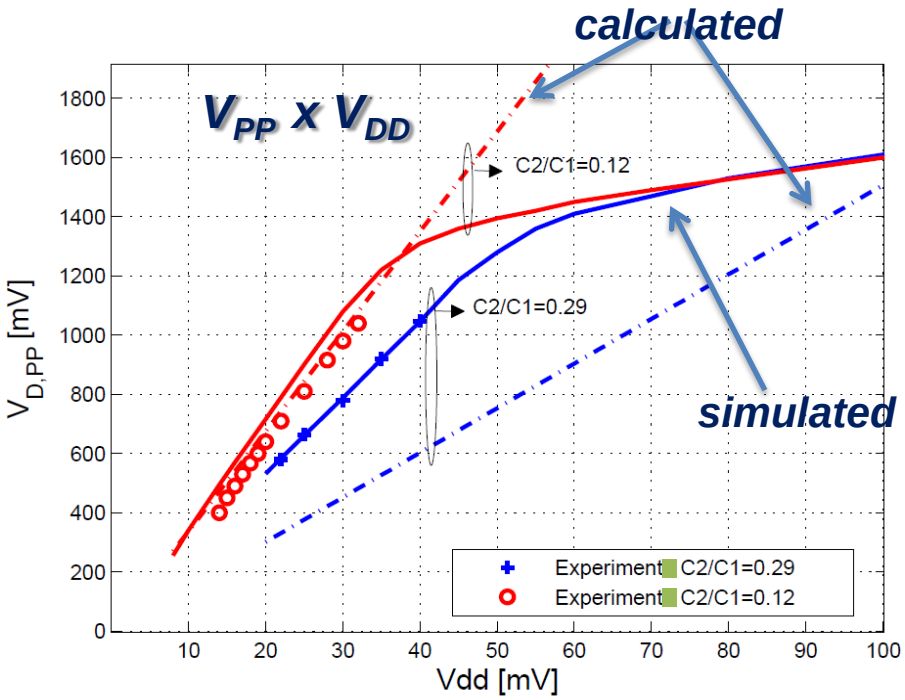


V_{PP}≈440 mV

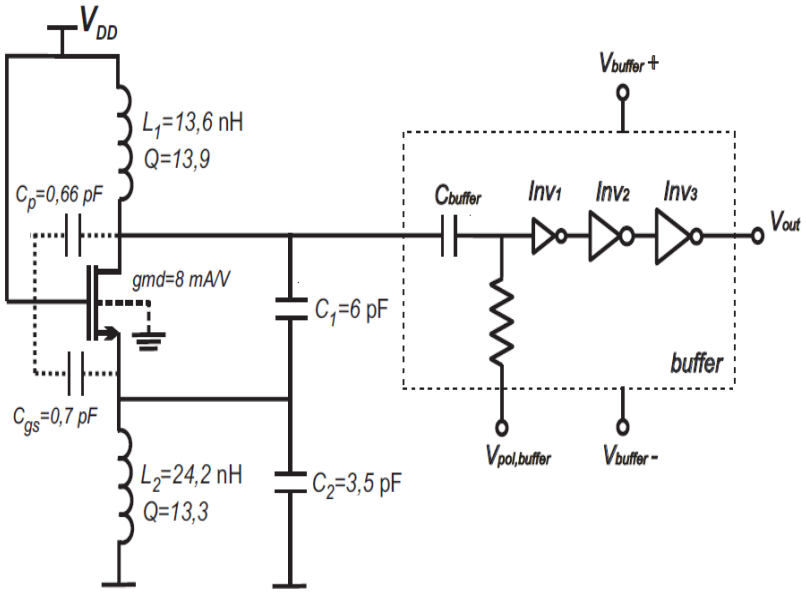
C2/C1=0.12

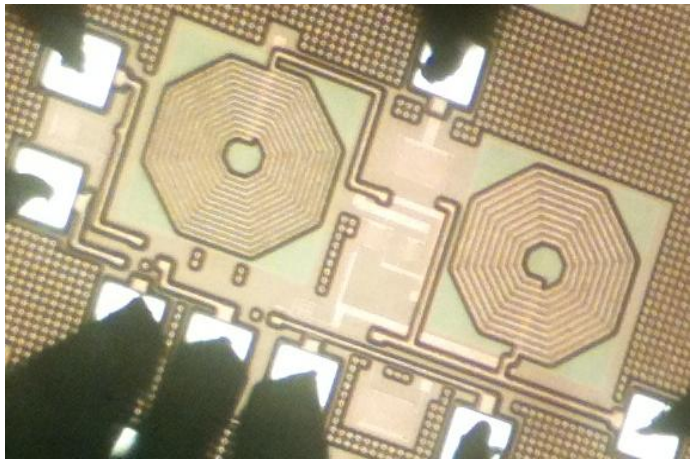
f_{osc}≈110 kHz

V_{DD}=15 mV

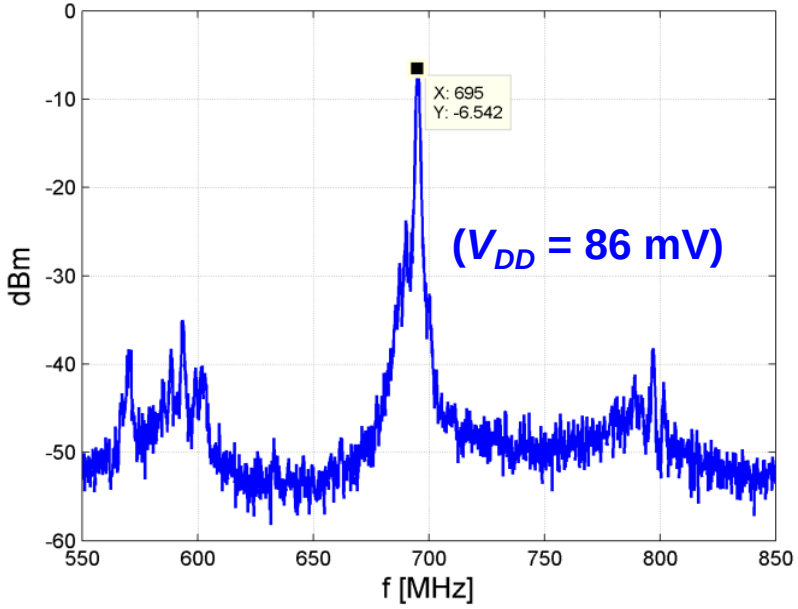


Colpitts oscillator – IC prototype

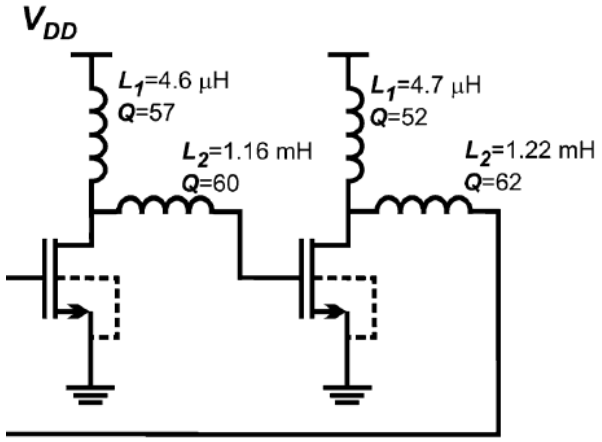


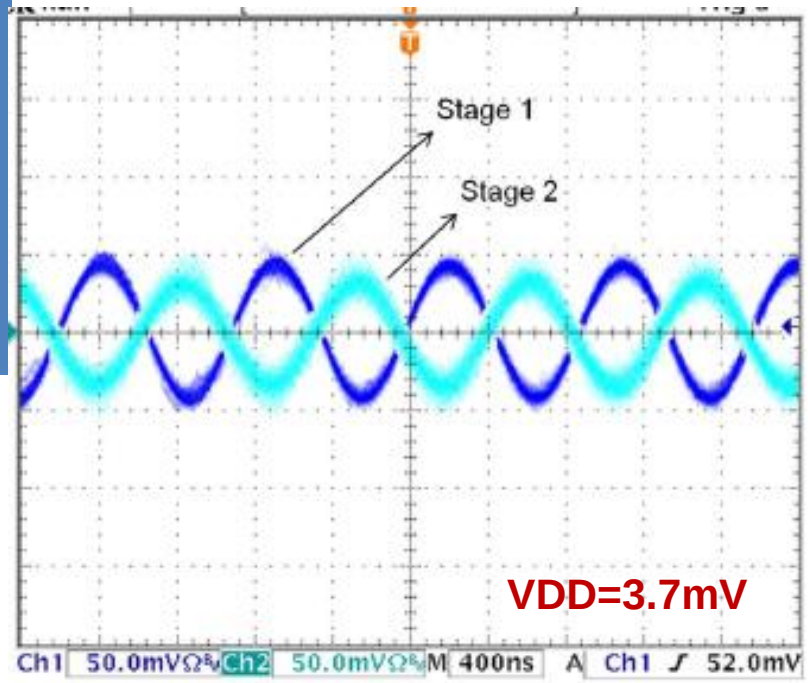


130 nm technology



Enhanced-swing ring oscillator (ESRO)





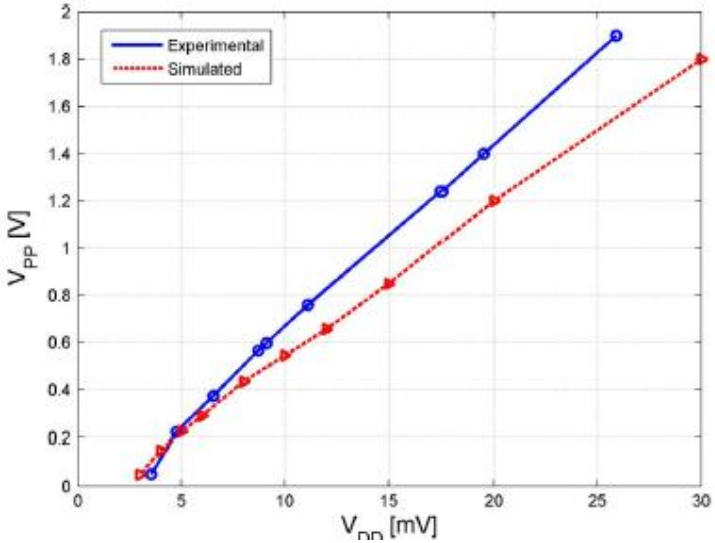
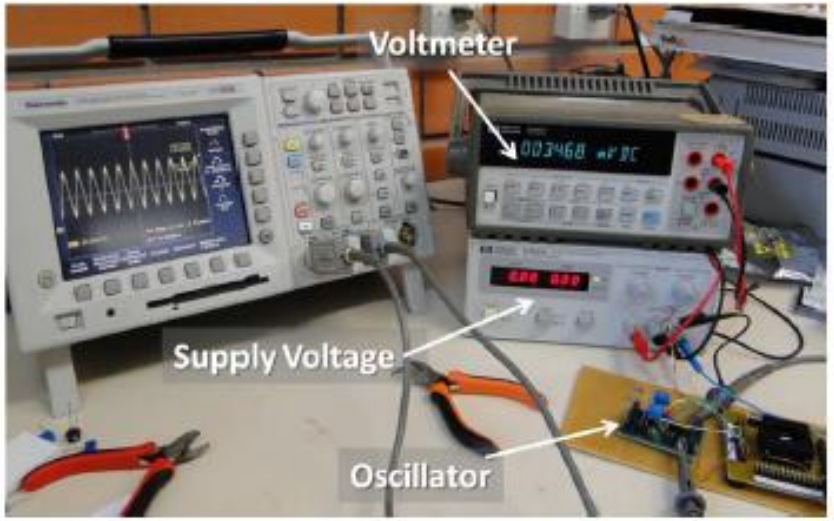


Fig. 12. Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage versus supply voltage of the ES inductive-load ring oscillator.



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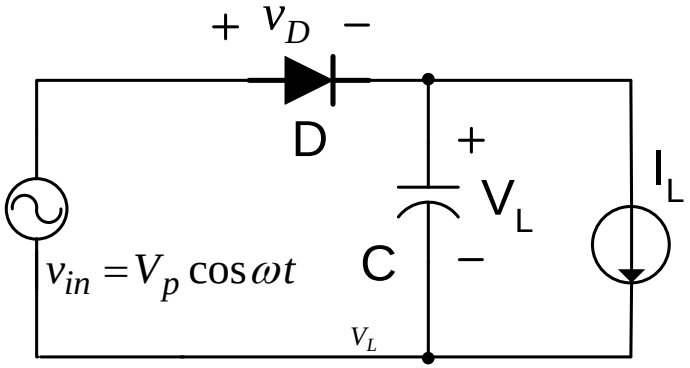
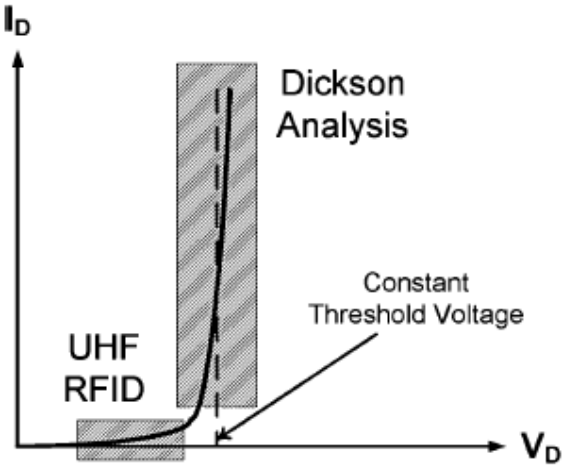
Ultra-low-voltage diode circuits

Dickson analysis of voltage multipliers: constant threshold voltage diode model, not appropriate for low voltage operation





$V_L = V_P - V_{ON}$

How to substitute the constant 'diode voltage drop' model?

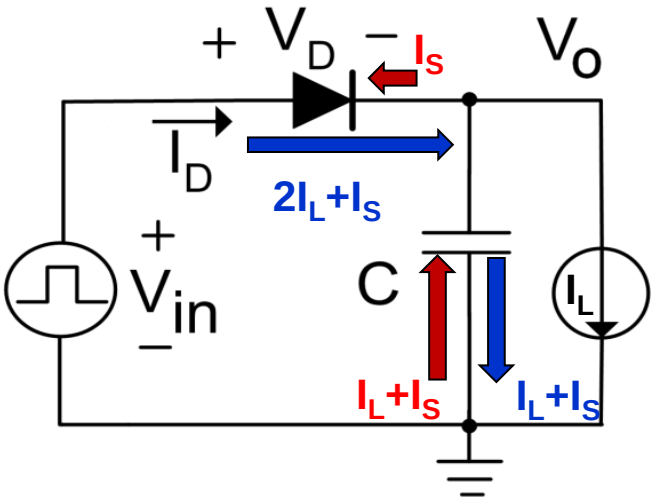
Use the i-v characteristic of the diode and the load current

$$I_D = I_S[e^{\frac{V_D}{n\phi_t}} - 1]$$

$$\phi_t = \frac{kT}{q}$$

$n \sim 1$ to 1.5

Single-stage voltage rectifier



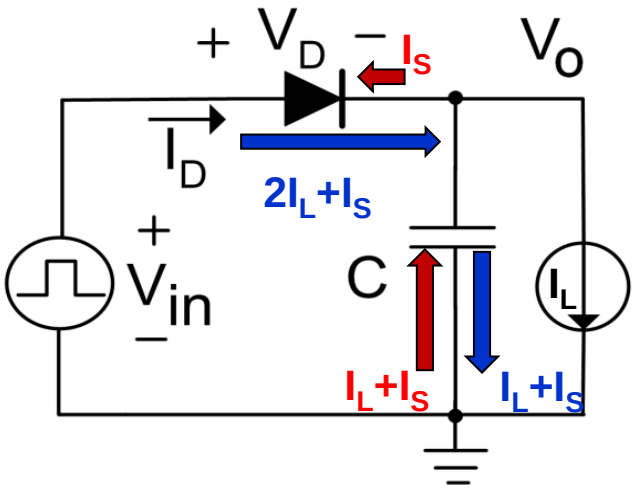
- Steady state analysis
- Low ripple
- Square wave input

$$\frac{1}{T}\int_{-T/2}^{T/2} I_D\,dt = \frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}-1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}-1\right)dt\right] = I_L$$

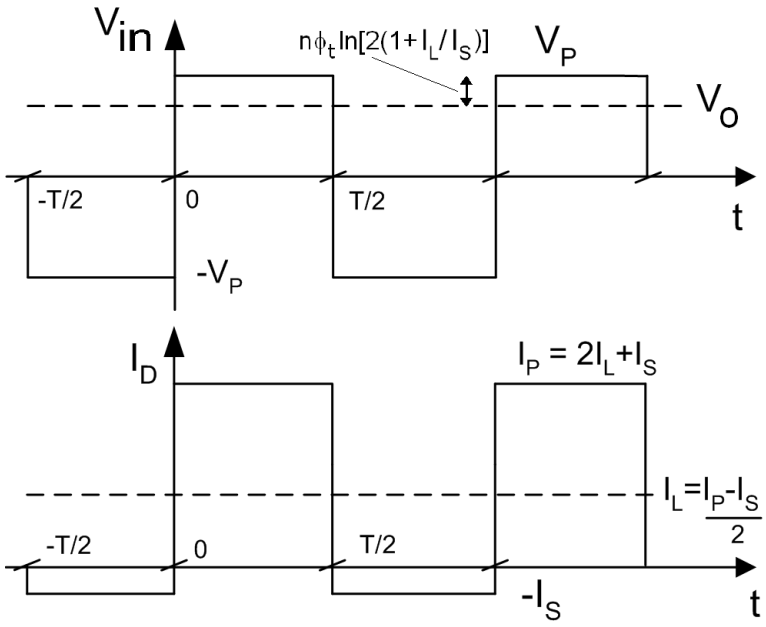
$$\frac{V_o}{n\phi_t} = \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_S}\right]$$

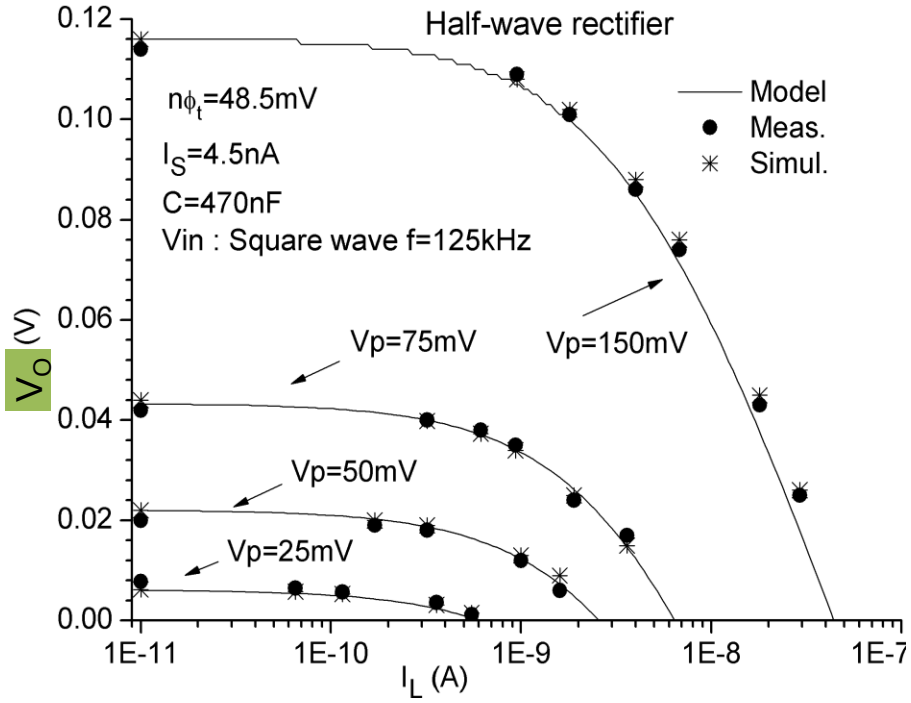
$$V_P > n\phi_t \Rightarrow V_o \cong V_P - n\phi_t \ln\left(2\left(1+\frac{I_L}{I_S}\right)\right) \longrightarrow \text{Diode "ON" voltage drop}$$

Single-stage voltage rectifier



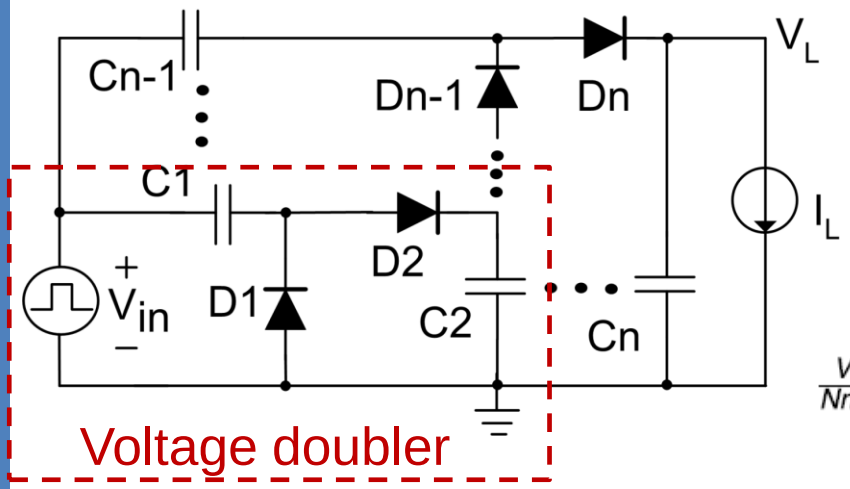
$$V_o \cong V_P - n\phi_t \ln\left(2\left(1+\frac{I_L}{I_S}\right)\right)$$





The voltage multiplier

N-stage voltage multiplier



Output voltage

$$\frac{V_L}{n\phi_t} = N \ln\left[\frac{I_0\left(V_A/n\phi_t\right)}{1 + I_L/I_S}\right]$$

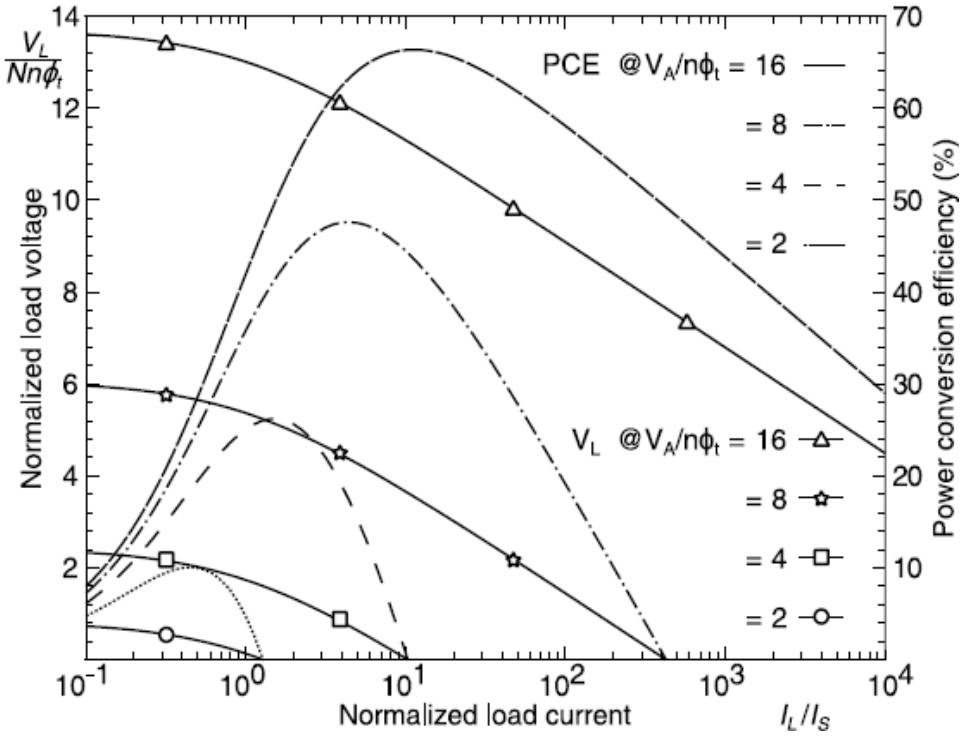
Modified Bessel function, first kind, order zero

Power conversion efficiency (PCE)

$$PCE = \frac{P_{load}}{P_{in}}$$

PCE is maximized for

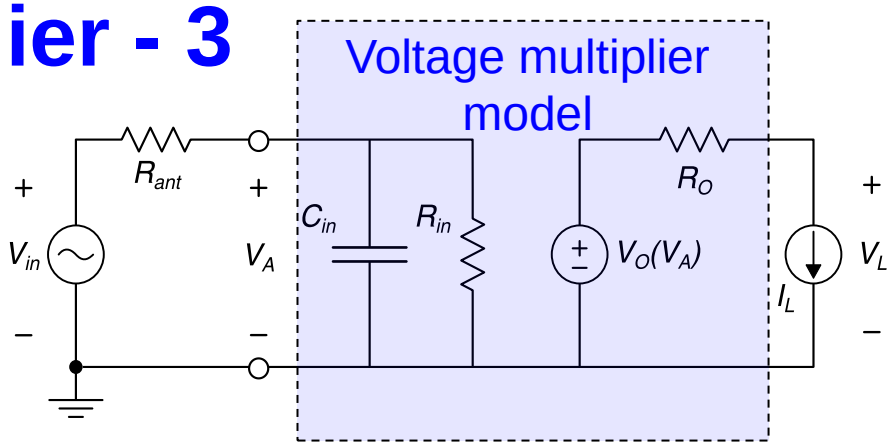
$$\frac{I_L}{I_S} = \frac{V_L}{Nn\phi_t}$$



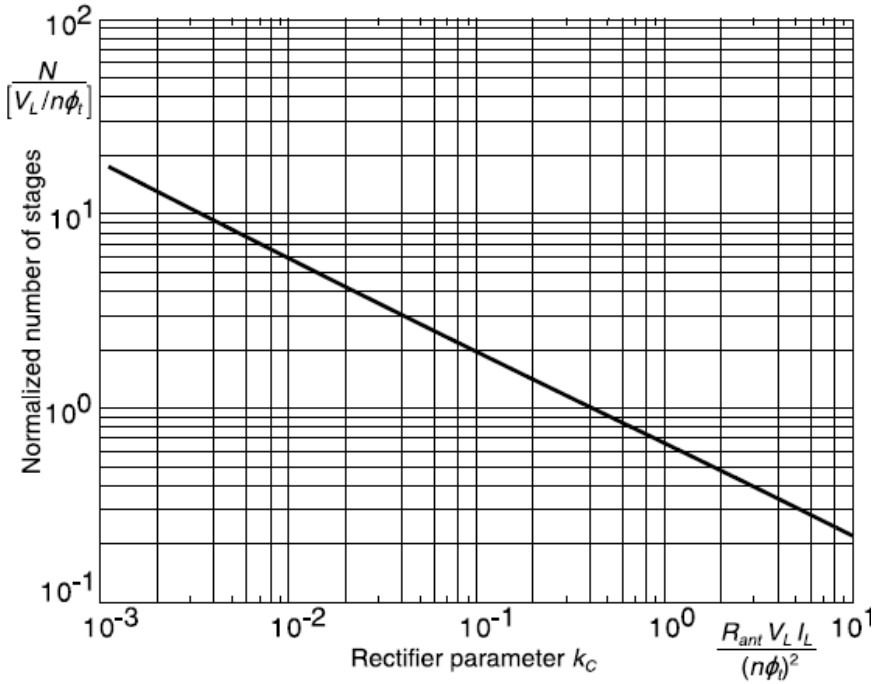
The voltage multiplier - 3

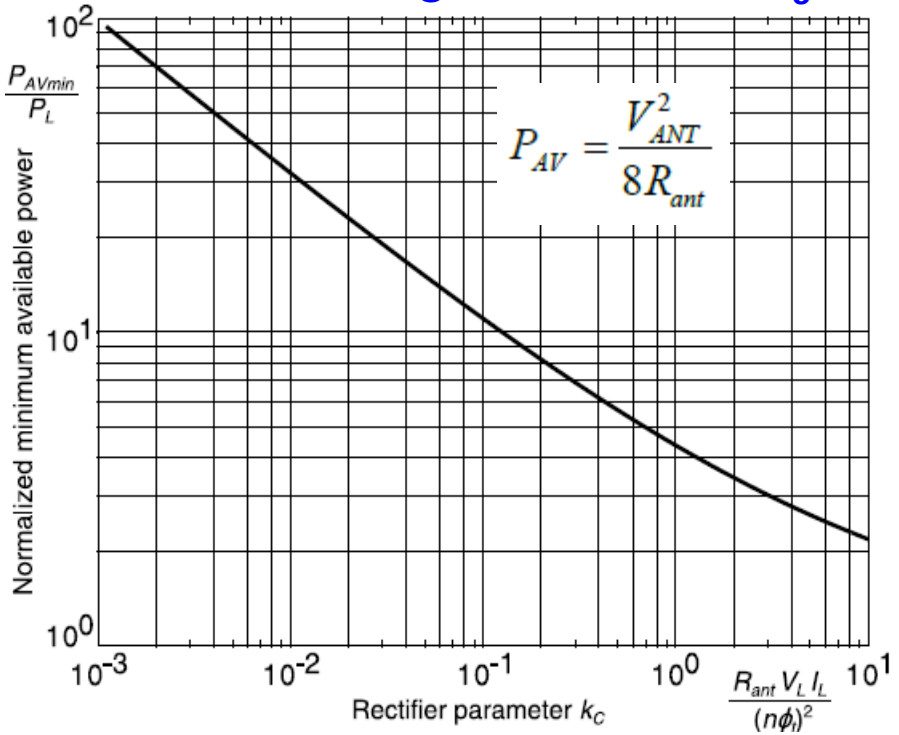
Model of the N-stage voltage multiplier

$$k_c = \frac{R_{ant} V_L I_L}{(n\phi_t)^2}$$

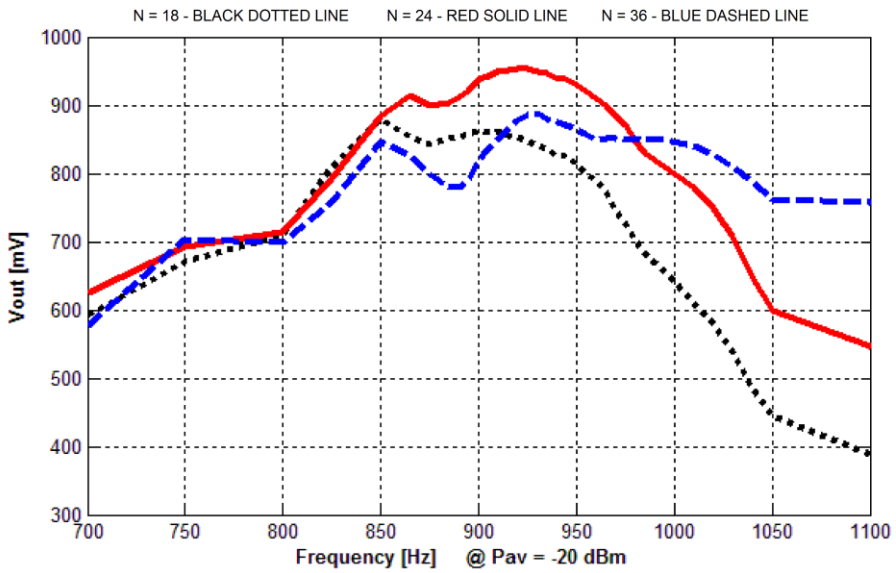


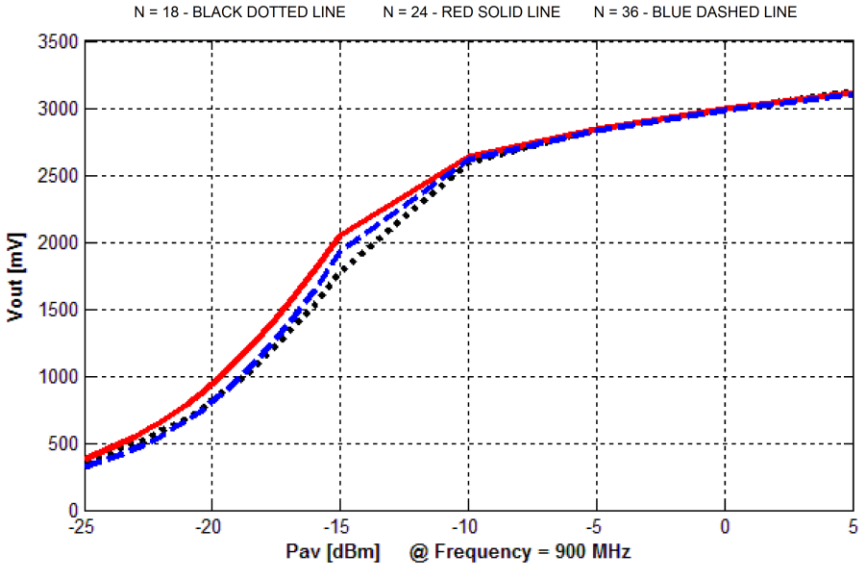
Design for minimum available power/maximum range in terms of k_c



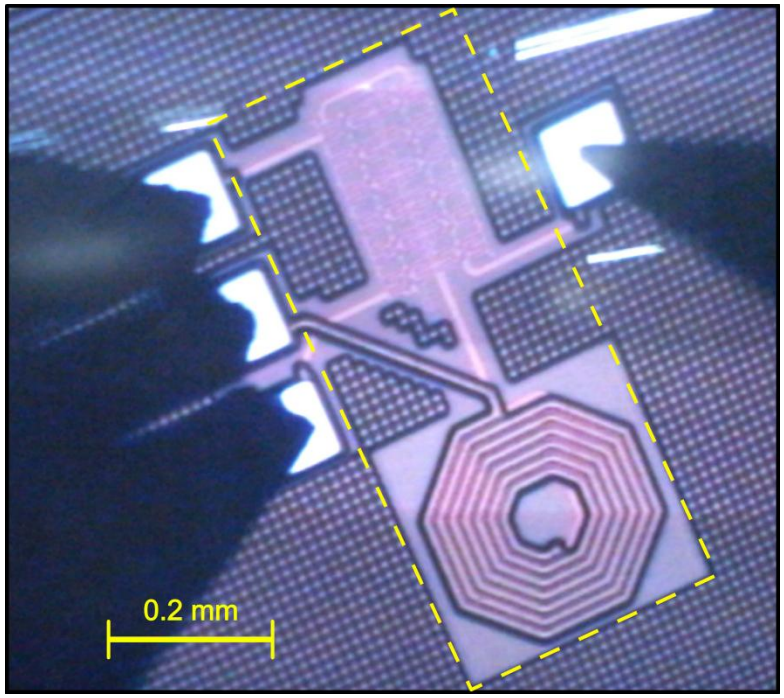


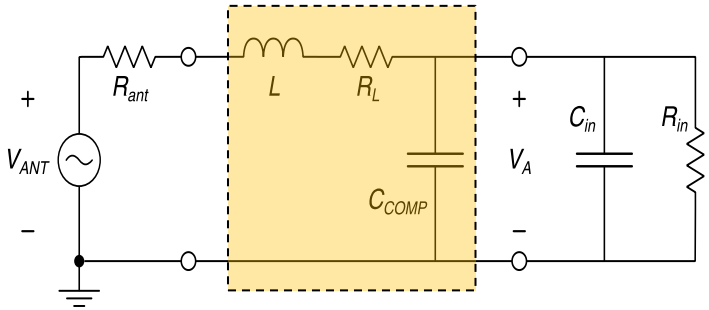
AC/DC converter in 130 nm CMOS technology





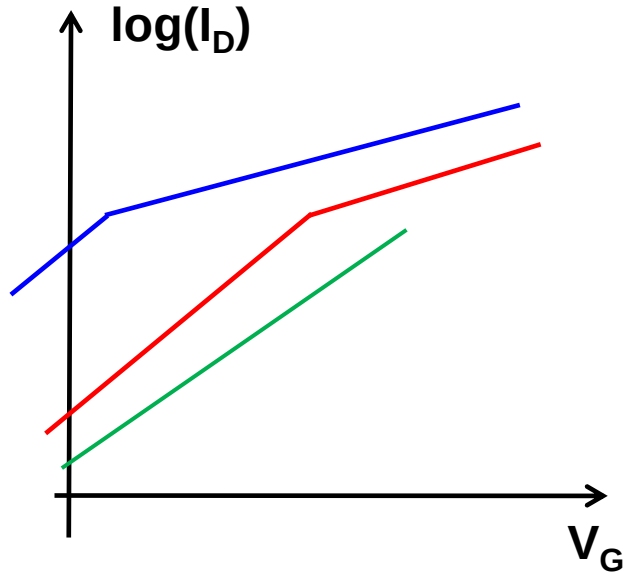
24-stage rectifier

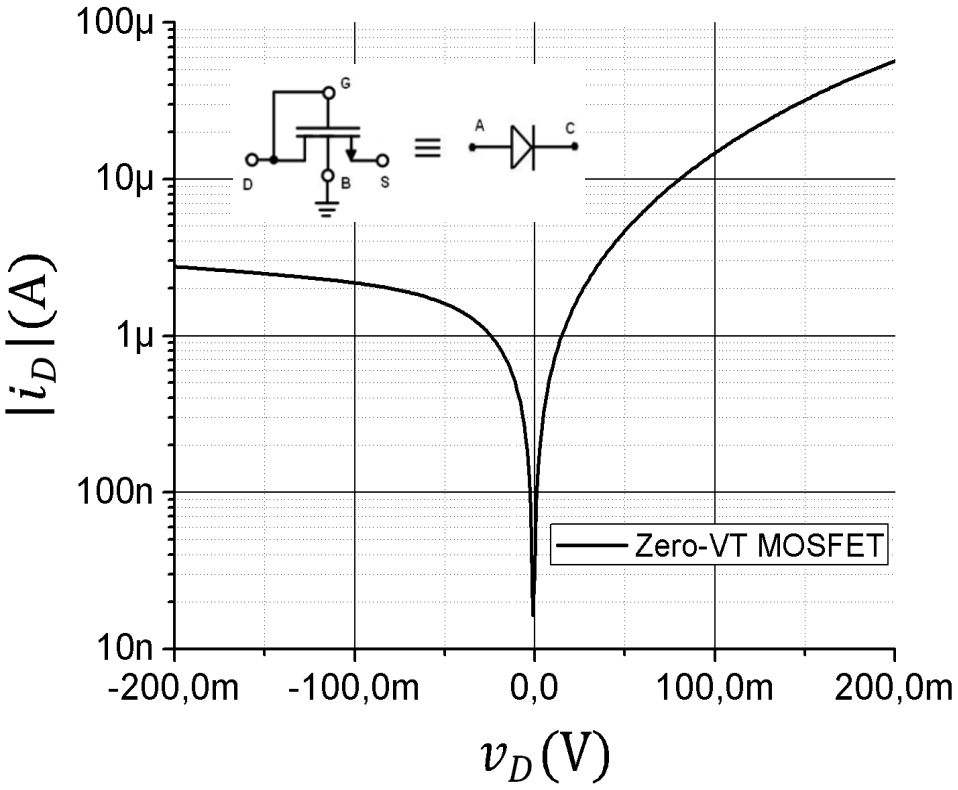




Matching network

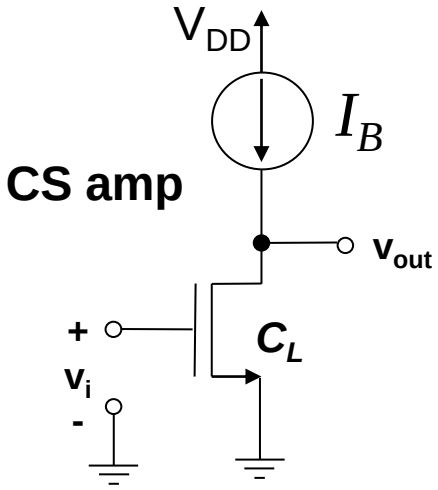
What about diodes?

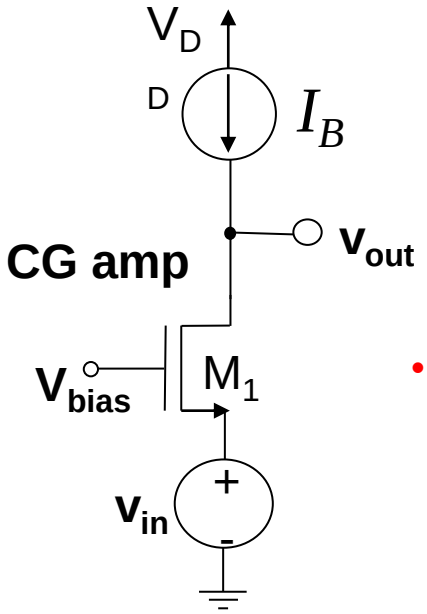


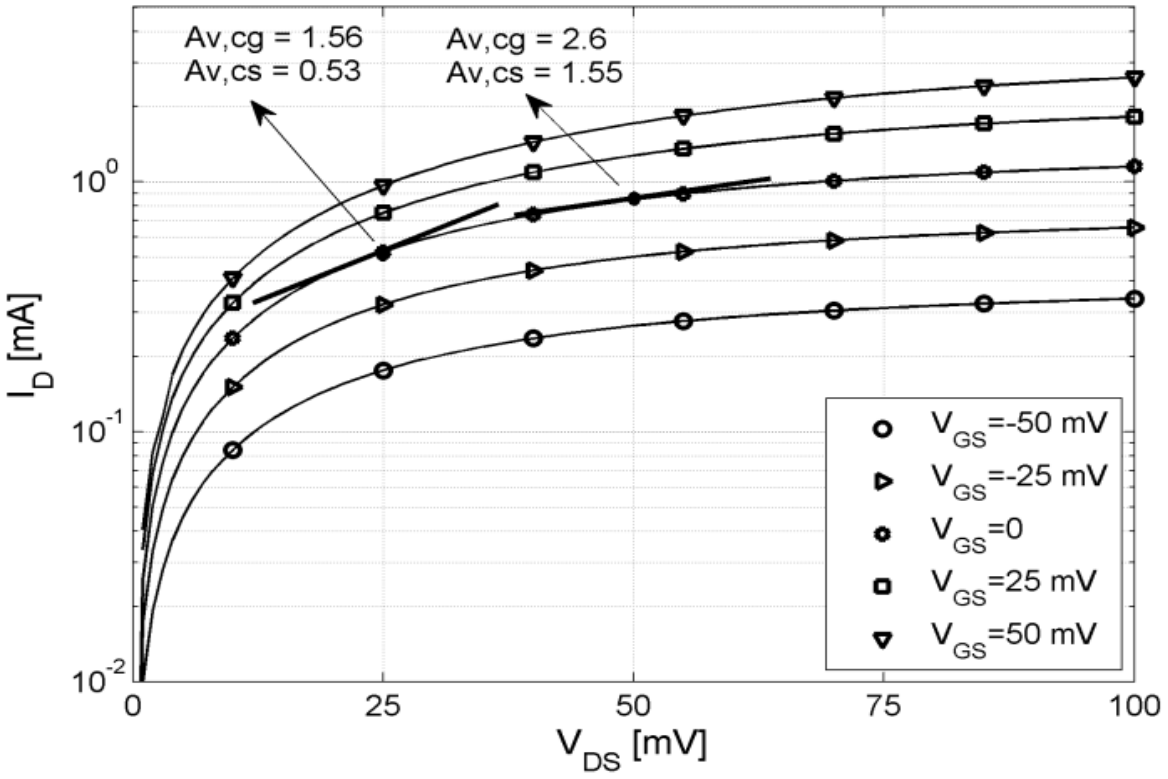


Diode-connected zero-VT MOSFET
- high drive capability (W/L≅7)

Zero-VT MOSFETs

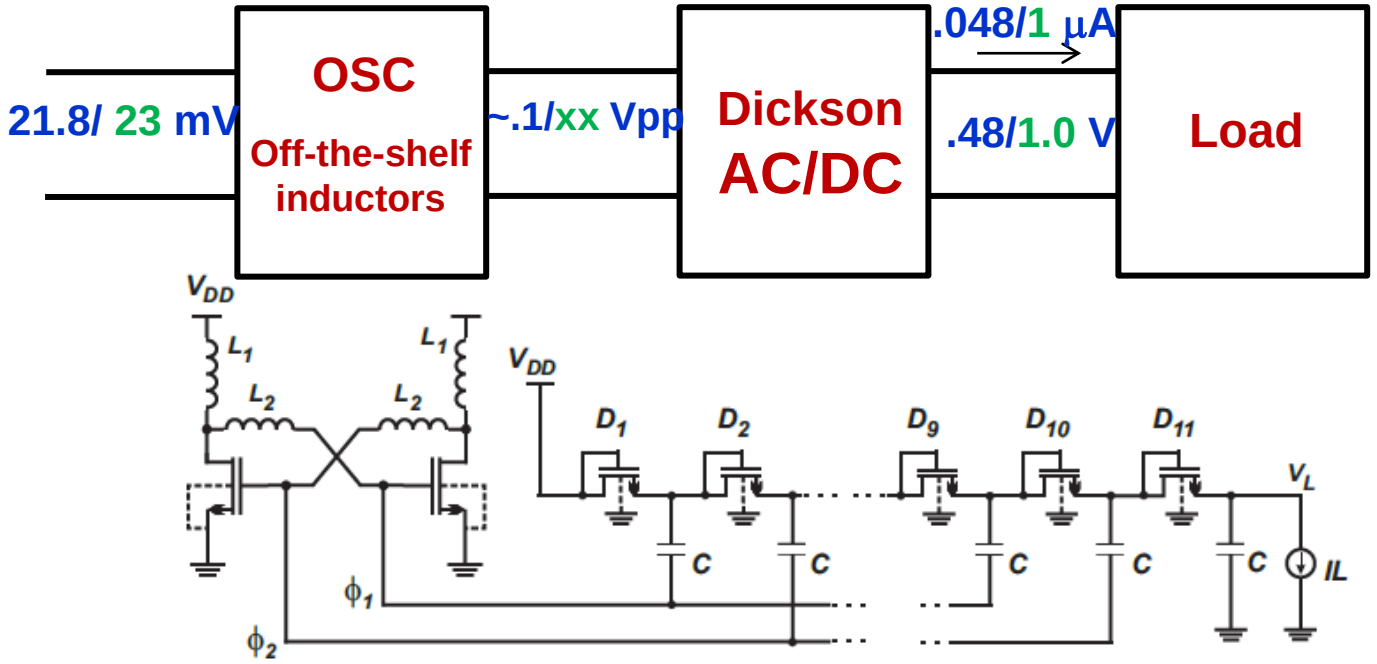


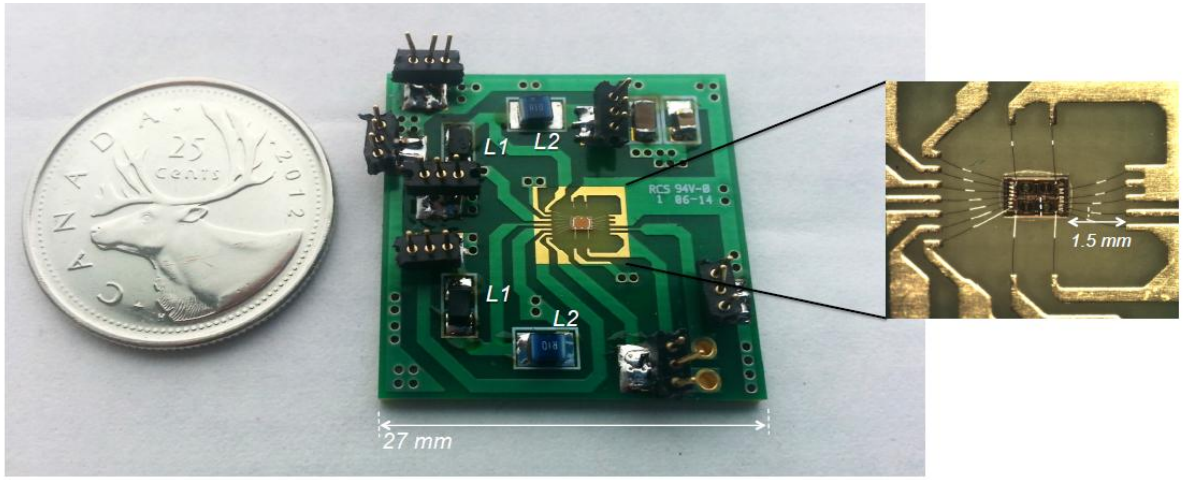




- I_D x V_{DS} (V_S=V_B) characteristics for a zero-VT transistor with W/L=2500µm/420nm. For V_{GS}= 0 V and V_{DS}= 25 mV the values of the common-gate and common-source gains are 1.56 and 0.53, respectively (moderate inversion operation).

Energy harvester





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